## SPEC® CPU2017 Integer Rate Result

**Cisco Systems**  
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Sponsor</th>
<th>Tested by</th>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
</table>

### SPECrate2017_int_base = 232  
### SPECrate2017_int_peak = Not Run

### Hardware
- **CPU Name:** Intel Xeon Gold 6240  
- **Max MHz.:** 3900  
- **Nominal:** 2600  
- **Enabled:** 36 cores, 2 chips, 2 threads/core  
- **Orderable:** 1,2 Chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **Cache L2:** 1 MB I+D on chip per core  
- **Cache L3:** 24.75 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
- **Storage:** 1 x 1.9 TB SSD SAS  
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.0.4c released Apr-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** None

---

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>72</td>
<td>0</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>72</td>
<td>185</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>72</td>
<td>151</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>72</td>
<td>312</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>72</td>
<td>261</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>72</td>
<td>459</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>72</td>
<td>199</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>72</td>
<td>255</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>72</td>
<td>423</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>72</td>
<td>153</td>
</tr>
</tbody>
</table>
### Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

**SPECrate2017_int_base = 232**

**SPECrate2017_int_peak = Not Run**

---

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>72</td>
<td>634</td>
<td>181</td>
<td><strong>632</strong></td>
<td>181</td>
<td>631</td>
<td>182</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>72</td>
<td>548</td>
<td>186</td>
<td><strong>550</strong></td>
<td>185</td>
<td>551</td>
<td>185</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>72</td>
<td><strong>373</strong></td>
<td><strong>312</strong></td>
<td>373</td>
<td>312</td>
<td>373</td>
<td>312</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>72</td>
<td>625</td>
<td>151</td>
<td><strong>626</strong></td>
<td>151</td>
<td>627</td>
<td>151</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>72</td>
<td>292</td>
<td>260</td>
<td>291</td>
<td>262</td>
<td><strong>292</strong></td>
<td><strong>261</strong></td>
</tr>
<tr>
<td>525.x264_r</td>
<td>72</td>
<td>275</td>
<td>459</td>
<td><strong>275</strong></td>
<td><strong>459</strong></td>
<td>275</td>
<td>458</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>72</td>
<td>416</td>
<td>199</td>
<td><strong>415</strong></td>
<td><strong>199</strong></td>
<td>415</td>
<td>199</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>72</td>
<td>643</td>
<td>186</td>
<td><strong>638</strong></td>
<td>187</td>
<td>631</td>
<td>189</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>72</td>
<td>446</td>
<td>423</td>
<td>446</td>
<td>423</td>
<td><strong>446</strong></td>
<td><strong>423</strong></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>72</td>
<td>508</td>
<td>153</td>
<td><strong>509</strong></td>
<td><strong>153</strong></td>
<td>509</td>
<td>153</td>
</tr>
</tbody>
</table>

---

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### General Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
```

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate2017_int_base = 232
SPECrate2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

General Notes (Continued)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcede8f2999c33d61f64985e45859ea9
running on linux-4z0x Thu May 23 02:56:54 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
  2 "physical id"s (chips)
  72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 36
  physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 2
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
Stepping: 6
CPU MHz: 2600.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000

(Continued on next page)
SPEC CPU2017 Integer Rate Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate2017_int_base = 232
SPECrate2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: May-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

Platform Notes (Continued)

BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-2,5,6,9,10,14,15,36-38,41,42,45,46,50,51
NUMA node1 CPU(s): 3,4,7,8,11-13,16,17,39,40,43,44,47-49,52,53
NUMA node2 CPU(s): 18-20,23,24,27,28,32,33,54-56,59,60,63,64,68,69
NUMA node3 CPU(s): 21,22,25,26,29-31,34,35,37,38,58,61,62,65-67,70,71
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 cflush dtst acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 sse3
sd sbg fma cx16 xtpdr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_13 invpcid_single intel_pinn tpr_shadow vmmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpd cd trt cqm mpx rdtn
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsavec qcm_llc qcm_occu_llc qcm_mmb_total qcm_mmb_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 6 9 10 14 15 36 37 38 41 42 45 46 50 51
node 0 size: 192073 MB
node 0 free: 189664 MB
node 1 cpus: 3 4 7 8 11 12 13 16 17 39 40 43 44 47 48 49 52 53
node 1 size: 193527 MB
node 1 free: 191351 MB
node 2 cpus: 18 19 20 23 24 27 28 32 33 54 55 56 59 60 63 64 68 69
node 2 size: 193527 MB
node 2 free: 191356 MB
node 3 cpus: 21 22 25 26 29 30 31 34 35 37 58 61 62 65 66 67 70 71
node 3 size: 193525 MB
node 3 free: 191213 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>232</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

From /proc/meminfo
MemTotal: 791197416 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*

os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-4z0x 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 May 22 17:55

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdaf1 xfs 891G 36G 856G 4% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.4c.0.0411190411 04/11/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate2017_int_base = 232
SPECrate2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

Compiler Version Notes
==============================================================================
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base)
    557.xz_r(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
    541.leela_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
FC  548.exchange2_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation
C benchmarks:
  icc -m64 -std=c11

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64

Base Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate2017_int_base = 232
SPECrate2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Base Portability Flags (Continued)

523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

SPEC is a registered trademark of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-05-22 17:26:53-0400.
Originally published on 2019-07-09.