SPEC® CPU2017 Floating Point Rate Result

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Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(3.00 GHz, Intel Xeon Gold 5217)

SPECRate2017_fp_base = 116
SPECRate2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name:</td>
<td>Intel Xeon Gold 5217</td>
</tr>
<tr>
<td>Max MHz.:</td>
<td>3700</td>
</tr>
<tr>
<td>Nominal:</td>
<td>3000</td>
</tr>
<tr>
<td>Enabled:</td>
<td>16 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1, 2 chip(s)</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
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<tr>
<td>L3:</td>
<td>11 MB I+D on chip per chip</td>
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<tr>
<td>Other:</td>
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</tr>
<tr>
<td>Memory:</td>
<td>384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R, running at 2666)</td>
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<tr>
<td>Storage:</td>
<td>1 x 400 GB SAS SSD, RAID 0</td>
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<tr>
<td>Other:</td>
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</tr>
<tr>
<td>OS:</td>
<td>SUSE Linux Enterprise Server 15 (x86_64)</td>
</tr>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.2.187 of Intel C/C++</td>
</tr>
<tr>
<td>Compiler Build:</td>
<td>20190117 for Linux;</td>
</tr>
<tr>
<td>Fortran:</td>
<td>Version 19.0.2.187 of Intel Fortran</td>
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<td>Compiler Build:</td>
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<tr>
<td>Parallel:</td>
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<tr>
<td>Firmware:</td>
<td>HPE BIOS Version I42 05/22/2019 released May-2019</td>
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<tr>
<td>File System:</td>
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</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
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<tr>
<td>Base Pointers:</td>
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<td>Peak Pointers:</td>
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<td>Other:</td>
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<tr>
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<tr>
<td>508.namd_r</td>
<td>63.5</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>76.8</td>
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<tr>
<td>521.wrf_r</td>
<td>114</td>
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<tr>
<td>527.cam4_r</td>
<td>177</td>
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<td>544.nab_r</td>
<td>57.8</td>
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<tr>
<td>554.roms_r</td>
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</table>

Test Date: Jun-2019
Hardware Availability: May-2019
Software Availability: Feb-2019

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

503.bwaves_r 32
507.cactuBSSN_r 32
508.namd_r 32
510.parest_r 32
511.povray_r 32
519.lbm_r 32
521.wrf_r 32
526.blender_r 32
527.cam4_r 32
538.imagick_r 32
544.nab_r 32
549.fotonik3d_r 32
554.roms_r 32

Intel Xeon Gold 5217
3.00 GHz, Intel Xeon Gold 5217
Synergy 480 Gen10
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Email: info@spec.org
Website: https://www.spec.org
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<td>881</td>
<td>57.7</td>
</tr>
</tbody>
</table>

**SPECrate2017_fp_base =** 116  
**SPECrate2017_fp_peak =** Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
    sync; echo 3 > /proc/sys/vm/drop_caches  
runcpu command invoked through numactl i.e.:  
    numactl --interleave=all runcpu <etc>

**General Notes**

Environment variables set by runcpu before the start of the run:  
LD_LIBRARY_PATH = "/home/cpu2017_u2/lib/ia32:/home/cpu2017_u2/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Configuration:
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Throughput Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Performance
Sysinfo program /home/cpu2017_u2/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on sy480g10-2 Thu Jun 27 22:52:35 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5217 CPU @ 3.00GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel

(Continued on next page)
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Test Sponsor: HPE
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Platform Notes (Continued)

CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5217 CPU @ 3.00GHz
Stepping: 6
CPU MHz: 3000.000
BogoMIPS: 6000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdkg fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

From /proc/cpuinfo

From /proc/meminfo

MemTotal: 395627144 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

(Continued on next page)
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</tbody>
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Platform Notes (Continued)

From /etc/*release* /etc/*version*

os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux sy480g10-2 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Jun 27 22:50

SPEC is set to: /home/cpu2017_u2

<table>
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<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sdb2</td>
<td>btrfs</td>
<td>371G</td>
<td>93G</td>
<td>278G</td>
<td>25%</td>
<td>/home</td>
</tr>
</tbody>
</table>

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS HPE I42 05/22/2019
Memory:
  24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933, configured at 2666

Compiler Version Notes

==============================================================================
CC  519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

(Continued on next page)
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**Tested by:** HPE  
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**Hardware Availability:** May-2019  
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**Compiler Version Notes (Continued)**

```plaintext
CXXC 508.namd_r(base) 510.parest_r(base)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

CC 511.povray_r(base) 526.blender_r(base)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

FC 507.cactuBSSN_r(base)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

FC 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

CC 521.wrf_r(base) 527.cam4_r(base)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
```

(Continued on next page)
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**Compiler Version Notes (Continued)**

64, Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel (R) C Intel (R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

**Base Compiler Invocation**

C benchmarks:
```plaintext
icc -m64 -std=c11
```

C++ benchmarks:
```plaintext
icpc -m64
```

Fortran benchmarks:
```plaintext
ifort -m64
```

Benchmarks using both Fortran and C:
```plaintext
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:
```plaintext
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```plaintext
icpc -m64 icc -m64 -std=c11 ifort -m64
```

---

**Base Portability Flags**

```plaintext
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```
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**Base Optimization Flags**

C benchmarks:
- `xCORE-AVX2 -ipo -o3 -no-prec-div -qopt-prefetch -ffinite-math-only`  
- `qopt-mem-layout-trans=4`

C++ benchmarks:
- `xCORE-AVX2 -ipo -o3 -no-prec-div -qopt-prefetch -ffinite-math-only`  
- `qopt-mem-layout-trans=4`

Fortran benchmarks:
- `xCORE-AVX2 -ipo -o3 -no-prec-div -qopt-prefetch -ffinite-math-only`  
- `qopt-mem-layout-trans=4`  
- `auto`  
- `nostandard-realloc-lhs`  
- `align array32byte`

Benchmarks using both Fortran and C:
- `xCORE-AVX2 -ipo -o3 -no-prec-div -qopt-prefetch -ffinite-math-only`  
- `qopt-mem-layout-trans=4`  
- `auto`  
- `nostandard-realloc-lhs`  
- `align array32byte`

Benchmarks using both C and C++:
- `xCORE-AVX2 -ipo -o3 -no-prec-div -qopt-prefetch -ffinite-math-only`  
- `qopt-mem-layout-trans=4`

Benchmarks using Fortran, C, and C++:
- `xCORE-AVX2 -ipo -o3 -no-prec-div -qopt-prefetch -ffinite-math-only`  
- `qopt-mem-layout-trans=4`  
- `auto`  
- `nostandard-realloc-lhs`  
- `align array32byte`

The flags files that were used to format this result can be browsed at:
- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html)

You can also download the XML flags sources by saving the following links:
- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml)

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**Original Publication:** July 30, 2019  
**Report Generation:** July 30, 2019 16:34:50  
**Software Used:** CPU2017 PDF formatter v6067

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**For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.**

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Tested with SPEC CPU2017 v1.0.5 on 2019-06-27 23:52:34-0400.  