Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5215, 2.50GHz)
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_r</td>
<td>40</td>
<td>690</td>
<td>92.2</td>
<td>692</td>
<td>92.0</td>
<td><strong>692</strong></td>
<td><strong>92.1</strong></td>
<td>40</td>
<td>603</td>
<td>106</td>
<td>606</td>
<td>105</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>gcc_r</td>
<td>40</td>
<td><strong>599</strong></td>
<td><strong>94.6</strong></td>
<td>596</td>
<td>95.1</td>
<td>599</td>
<td>94.5</td>
<td>40</td>
<td>510</td>
<td>111</td>
<td>511</td>
<td>111</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mcf_r</td>
<td>40</td>
<td>412</td>
<td>157</td>
<td>415</td>
<td>156</td>
<td><strong>415</strong></td>
<td><strong>156</strong></td>
<td>40</td>
<td>414</td>
<td>156</td>
<td>415</td>
<td>156</td>
<td>413</td>
<td>156</td>
<td></td>
<td></td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>40</td>
<td><strong>683</strong></td>
<td><strong>76.9</strong></td>
<td>683</td>
<td>76.9</td>
<td>682</td>
<td>76.9</td>
<td>40</td>
<td>682</td>
<td>77.0</td>
<td>684</td>
<td>76.7</td>
<td><strong>682</strong></td>
<td><strong>76.9</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>40</td>
<td>329</td>
<td>128</td>
<td>328</td>
<td>129</td>
<td>327</td>
<td>129</td>
<td>40</td>
<td>298</td>
<td>142</td>
<td>297</td>
<td>142</td>
<td>298</td>
<td>142</td>
<td></td>
<td></td>
</tr>
<tr>
<td>x264_r</td>
<td>40</td>
<td><strong>299</strong></td>
<td><strong>234</strong></td>
<td>298</td>
<td>235</td>
<td>301</td>
<td>232</td>
<td>40</td>
<td>287</td>
<td>244</td>
<td>287</td>
<td>244</td>
<td>286</td>
<td>245</td>
<td></td>
<td></td>
</tr>
<tr>
<td>deepsjeng_r</td>
<td>40</td>
<td>453</td>
<td>101</td>
<td>453</td>
<td>101</td>
<td>454</td>
<td>101</td>
<td>40</td>
<td>452</td>
<td>101</td>
<td>454</td>
<td>101</td>
<td><strong>453</strong></td>
<td><strong>101</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>leela_r</td>
<td>40</td>
<td><strong>713</strong></td>
<td><strong>92.9</strong></td>
<td>709</td>
<td>93.4</td>
<td>713</td>
<td>92.9</td>
<td><strong>40</strong></td>
<td><strong>714</strong></td>
<td><strong>92.8</strong></td>
<td>713</td>
<td>92.9</td>
<td>715</td>
<td>92.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>exchange2_r</td>
<td>40</td>
<td>426</td>
<td>246</td>
<td>426</td>
<td>246</td>
<td>427</td>
<td>246</td>
<td>40</td>
<td>426</td>
<td>246</td>
<td>427</td>
<td>246</td>
<td><strong>426</strong></td>
<td><strong>246</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>xz_r</td>
<td>40</td>
<td><strong>549</strong></td>
<td><strong>78.7</strong></td>
<td>549</td>
<td>78.7</td>
<td>549</td>
<td>78.7</td>
<td>40</td>
<td>548</td>
<td>78.8</td>
<td>550</td>
<td>78.6</td>
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</tr>
</tbody>
</table>

**Results appear in the order in which they were run. Bold underlined text indicates a median measurement.**

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
```

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
**SPEC CPU®2017 Integer Rate Result**

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 5215, 2.50GHz)

**SPECrate®2017_int_base = 119**

**SPECrate®2017_int_peak = 124**

<table>
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<td>Hardware Availability:</td>
<td>Apr-2019</td>
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<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
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</tbody>
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**General Notes (Continued)**

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

**Platform Notes**

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-4.15.5 Tue Aug 13 17:05:55 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 5215 CPU @ 2.50GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 10
  siblings : 20
  physical 0: cores 0 1 2 3 4 8 9 10 11 12
  physical 1: cores 0 1 2 3 4 8 9 10 11 12
```

From lscpu:

```
Architecture:      x86_64
CPU op-mode(s):    32-bit, 64-bit
Byte Order:        Little Endian
CPU(s):            40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s):         2
NUMA node(s):      2
Vendor ID:         GenuineIntel
CPU family:        6
Model:             85
Model name:        Intel(R) Xeon(R) Gold 5215 CPU @ 2.50GHz
Stepping:          6
CPU MHz:           2500.000
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5215, 2.50GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

CPU max MHz: 3400.0000
CPU min MHz: 1000.0000
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9,20-29
NUMA node1 CPU(s): 10-19,30-39
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperp tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sbfg fma cx16 xtpz pdcm pcdl dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_i3 cdpl3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pin pts pku ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
  node 0 size: 386549 MB
  node 0 free: 386023 MB
  node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
  node 1 size: 387056 MB
  node 1 free: 386517 MB
  node distances: node 0 1: 10 21

From /proc/meminfo
  MemTotal: 792171804 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5215, 2.50GHz)

**SPEC CPU®2017 Integer Rate Result**

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<td>Software Availability: May-2019</td>
</tr>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Tested by: Cisco Systems</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

```
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

uname -a:
```
Linux linux-4vt5 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- **CVE-2017-5754** (Meltdown): Not affected
- **CVE-2017-5753** (Spectre variant 1): Mitigation: __user pointer sanitization
- **CVE-2017-5715** (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 13 16:57

SPEC is set to: /home/cpu2017
```
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 224G 20G 204G 9% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

**BIOS** Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019

**Memory:**
```
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666
```

(End of data from sysinfo program)

**Compiler Version Notes**

```
C  | 502.gcc_r(peak)
```

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5215, 2.50GHz)

SPEC CPU®2017 Integer Rate Result

SPECrates®

SPECrates®2017_int_base = 119
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

C

| 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C

| 502.gcc_r(peak)

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C

| 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++

| 523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++

| 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++

| 523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416

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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5215, 2.50GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 119
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Compiler Version Notes (Continued)
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
       | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation
C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
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Cisco UCS C240 M5 (Intel Xeon Gold 5215, 2.50GHz)

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</table>

### Base Optimization Flags

**C benchmarks:**
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

**C++ benchmarks:**
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

**Fortran benchmarks:**
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-nostandard-realloc-lhs`
- `-align array32byte`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

### Peak Compiler Invocation

**C benchmarks (except as noted below):**
- `icc -m64 -std=c11`

**C++ benchmarks (except as noted below):**
- `icpc -m64`
- `523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin`

**Fortran benchmarks:**
- `ifort -m64`

### Peak Portability Flags

- `500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64`
- `502.gcc_r: -D_FILE_OFFSET_BITS=64`
- `505.mcf_r: -DSPEC_LP64`
- `520.omnetpp_r: -DSPEC_LP64`
- `523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX`
- `525.x264_r: -DSPEC_LP64`

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**Peak Portability Flags (Continued)**

531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

**Peak Optimization Flags**

**C benchmarks:**

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-fno-strict-overflow  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -fno-alias  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

557.xz_r: Same as 505.mcf_r

**C++ benchmarks:**

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

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</table>

**Peak Optimization Flags (Continued)**

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
-`-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`  
-`-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
-`-lqkmalloc`  

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-08-13 07:35:54-0400.  
Originally published on 2019-09-06.