## Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5222, 3.80GHz)

**SPECrates**:
- **SPECrater2017_fp_base = 78.1**
- **SPECrater2017_fp_peak = 79.3**

### CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

### Test Details
- **Test Date:** Aug-2019
- **Hardware Availability:** Apr-2019
- **Software Availability:** May-2019

### Hardware Details
- **CPU Name:** Intel Xeon Gold 5222
  - Max MHz: 3900
  - Nominal: 3800
  - Enabled: 8 cores, 2 chips, 2 threads/core
  - Orderable: 1,2 Chips
  - Cache L1: 32 KB I + 32 KB D on chip per core
  - L2: 1 MB I+D on chip per core
  - L3: 16.5 MB I+D on chip per core
  - Other: None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2934)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Software Details
- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
  - 4,12-14-23-default
- **Compiler:**
  - C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux
  - Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4d released May-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** --

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### SPEC CPU2017 Floating Point Rate Result

#### Copies

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate2017_fp_peak</th>
<th>SPECrate2017_fp_base</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>16</td>
<td>47.2</td>
<td>47.2</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>16</td>
<td>48.1</td>
<td>48.3</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>16</td>
<td>59.3</td>
<td>59.3</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>16</td>
<td>73.8</td>
<td>84.9</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>16</td>
<td>49.2</td>
<td>91.8</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>16</td>
<td>67.4</td>
<td>94.1</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>16</td>
<td>67.4</td>
<td>77.4</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>16</td>
<td>78.7</td>
<td>151</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>16</td>
<td>72.9</td>
<td>103</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>16</td>
<td>72.9</td>
<td>103</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>16</td>
<td>72.9</td>
<td>103</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>16</td>
<td>52.9</td>
<td>54.0</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>16</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

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<td>16</td>
<td>48.1</td>
<td>48.3</td>
</tr>
<tr>
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<td>16</td>
<td>59.3</td>
<td>59.3</td>
</tr>
<tr>
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<td>16</td>
<td>73.8</td>
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</tr>
<tr>
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</tr>
<tr>
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<td>67.4</td>
<td>94.1</td>
</tr>
<tr>
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<td>16</td>
<td>67.4</td>
<td>77.4</td>
</tr>
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<td>16</td>
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<td>151</td>
</tr>
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<td>103</td>
</tr>
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<td>16</td>
<td>72.9</td>
<td>103</td>
</tr>
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<td>16</td>
<td>72.9</td>
<td>103</td>
</tr>
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<td>16</td>
<td>52.9</td>
<td>54.0</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>16</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>16</td>
<td>558</td>
<td>288</td>
<td>561</td>
<td>286</td>
<td>558</td>
<td>288</td>
<td>16</td>
<td>558</td>
<td>288</td>
<td>559</td>
<td>287</td>
<td>557</td>
<td>288</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>16</td>
<td>430</td>
<td>47.2</td>
<td>429</td>
<td>47.2</td>
<td>429</td>
<td>47.2</td>
<td>16</td>
<td>429</td>
<td>47.2</td>
<td>430</td>
<td>47.1</td>
<td>429</td>
<td>47.2</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>16</td>
<td>316</td>
<td>48.1</td>
<td>318</td>
<td>47.9</td>
<td>316</td>
<td>48.1</td>
<td>16</td>
<td>315</td>
<td>48.2</td>
<td>315</td>
<td>48.3</td>
<td>315</td>
<td>48.3</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>16</td>
<td>707</td>
<td>59.2</td>
<td>704</td>
<td>59.4</td>
<td>706</td>
<td>59.3</td>
<td>16</td>
<td>708</td>
<td>59.1</td>
<td>706</td>
<td>59.3</td>
<td>705</td>
<td>59.4</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>16</td>
<td>506</td>
<td>73.8</td>
<td>506</td>
<td>73.8</td>
<td>506</td>
<td>73.8</td>
<td>16</td>
<td>438</td>
<td>85.3</td>
<td>440</td>
<td>84.9</td>
<td>441</td>
<td>84.7</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>16</td>
<td>343</td>
<td>49.2</td>
<td>343</td>
<td>49.2</td>
<td>343</td>
<td>49.2</td>
<td>16</td>
<td>342</td>
<td>49.3</td>
<td>343</td>
<td>49.2</td>
<td>342</td>
<td>49.2</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>16</td>
<td>390</td>
<td>91.9</td>
<td>394</td>
<td>90.9</td>
<td>390</td>
<td>91.8</td>
<td>16</td>
<td>381</td>
<td>94.1</td>
<td>382</td>
<td>93.8</td>
<td>380</td>
<td>94.2</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>16</td>
<td>360</td>
<td>67.6</td>
<td>362</td>
<td>67.3</td>
<td>361</td>
<td>67.4</td>
<td>16</td>
<td>361</td>
<td>67.4</td>
<td>361</td>
<td>67.5</td>
<td>362</td>
<td>67.4</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>16</td>
<td>358</td>
<td>78.2</td>
<td>362</td>
<td>77.4</td>
<td>365</td>
<td>76.7</td>
<td>16</td>
<td>355</td>
<td>78.7</td>
<td>357</td>
<td>78.3</td>
<td>353</td>
<td>79.2</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>16</td>
<td>263</td>
<td>151</td>
<td>266</td>
<td>149</td>
<td>263</td>
<td>151</td>
<td>16</td>
<td>266</td>
<td>149</td>
<td>267</td>
<td>149</td>
<td>264</td>
<td>151</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>16</td>
<td>262</td>
<td>103</td>
<td>265</td>
<td>102</td>
<td>262</td>
<td>103</td>
<td>16</td>
<td>262</td>
<td>103</td>
<td>262</td>
<td>103</td>
<td>266</td>
<td>101</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>16</td>
<td>854</td>
<td>73.0</td>
<td>856</td>
<td>72.9</td>
<td>856</td>
<td>72.8</td>
<td>16</td>
<td>852</td>
<td>73.2</td>
<td>855</td>
<td>72.9</td>
<td>856</td>
<td>72.8</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>16</td>
<td>484</td>
<td>52.5</td>
<td>481</td>
<td>52.9</td>
<td>469</td>
<td>54.2</td>
<td>16</td>
<td>469</td>
<td>54.2</td>
<td>471</td>
<td>54.0</td>
<td>471</td>
<td>54.0</td>
</tr>
</tbody>
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**SPECrate®2017_fp_base = 78.1**  
**SPECrate®2017_fp_peak = 79.3**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

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### Submit Notes

The `numactl` mechanism was used to bind copies to processors. The config file option 'submit' was used to generate `numactl` commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by `runcpu` before the start of the run:  
`LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"`

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to `runcpu` invocation  
Filesystem page cache synced and cleared with:  
`sync; echo 3> /proc/sys/vm/drop_caches`  
`runcpu` command invoked through `numactl` i.e.:  
`numactl --interleave=all runcpu <etc>`

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECrate®2017_fp_base = 78.1
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcede8f29999c3d61f64985e45859ea9
running on linux-3c6s Wed Aug 14 04:59:12 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 5222 CPU @ 3.80GHz
    2 "physical id"s (chips)
    16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 8
physical 0: cores 2 5 9 13
physical 1: cores 2 5 8 12

From lscpu:
    Architecture: x86_64
    CPU op-mode(s): 32-bit, 64-bit
    Byte Order: Little Endian
    CPU(s): 16
    On-line CPU(s) list: 0-15
    Thread(s) per core: 2
    Core(s) per socket: 4
    Socket(s): 2
    NUMA node(s): 4
    Vendor ID: GenuineIntel
    CPU family: 6
    Model: 85
    Model name: Intel(R) Xeon(R) Gold 5222 CPU @ 3.80GHz
    Stepping: 6

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 5222, 3.80GHz)

<table>
<thead>
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</tr>
</thead>
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<td>Test Sponsor:</td>
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</tr>
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</tr>
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<td>SPECrate®2017_fp_base</td>
<td>78.1</td>
</tr>
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</tr>
</tbody>
</table>

### Platform Notes (Continued)

```plaintext
CPU MHz: 3800.000
CPU max MHz: 3900.0000
CPU min MHz: 1200.0000
BogoMIPS: 7600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 16896K
NUMA node0 CPU(s): 0,2,8,10
NUMA node1 CPU(s): 1,3,9,11
NUMA node2 CPU(s): 4,6,12,14
NUMA node3 CPU(s): 5,7,13,15
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pmm tpr_shadow vmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves cmp_legacy cmp_legacy_all cmp_legacy32 all_cmp_shadow all_cmp last_cmp wdt xsaveopt xsaves cmp_legacy cmp_legacy_all cmp_legacy32 all_cmp_shadow all_cmp last_cmp bbr wdt xsaveopt xsaves cmp_legacy cmp_legacy_all cmp_legacy32 all_cmp_shadow all_cmp last_cmp
```

From `numactl --hardware`:

```plaintext
WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

```plaintext
/proc/cpuinfo cache data
cache size : 16896 KB
```

(Continued on next page)
Cisco Systems
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SPECrate®2017_fp_peak = 79.3

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791208148 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-3c6s 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 13 22:28

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 224G 31G 193G 14% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is intended to allow hardware to be accurately determined, but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
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Compiler Version Notes

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</tr>
</thead>
<tbody>
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<td>Intel(R) C Intel(R) 64 Compiler</td>
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</tr>
<tr>
<td></td>
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<td></td>
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</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fortran</td>
<td>Intel(R) Fortran Intel(R) 64 Compiler</td>
<td>503.bwaves_r(base, peak)</td>
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</tr>
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</tr>
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Compiler Version Notes (Continued)

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
==============================================================================

Compiler Version Notes (Continued)

64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

### Cisco Systems

**Cisco UCS C240 M5** (Intel Xeon Gold 5222, 3.80GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>78.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>79.3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date</td>
<td>Aug-2019</td>
</tr>
<tr>
<td>Hardware Availability</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### Base Portability Flags (Continued)

- **521.wrf_r**: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- **526.blender_r**: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- **527.cam4_r**: -DSPEC_LP64 -DSPEC_CASE_FLAG
- **538.imagick_r**: -DSPEC_LP64
- **544.nab_r**: -DSPEC_LP64
- **549.fotonik3d_r**: -DSPEC_LP64
- **554.roms_r**: -DSPEC_LP64

### Base Optimization Flags

#### C benchmarks:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

#### C++ benchmarks:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

#### Fortran benchmarks:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

#### Benchmarks using both Fortran and C:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

#### Benchmarks using both C and C++:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

#### Benchmarks using Fortran, C, and C++:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

### Peak Compiler Invocation

C benchmarks:
- icc -m64 -std=c11

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECraten®2017_fp_base = 78.1
SPECraten®2017_fp_peak = 79.3

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5222, 3.80GHz)  

| SPECrate®2017_fp_base = 78.1 |
| SPECrate®2017_fp_peak = 79.3 |

CPU2017 License: 9019  
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Peak Optimization Flags (Continued)

Fortran benchmarks:

503.bwaves_r -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -auto  
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs  
-align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs  
-align array32byte

Benchmarks using both C and C++:

511.povray_r -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4

526.blender_r -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4  
-auto -nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4  
-auto -nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECrate\textsuperscript{\textregistered}2017\_fp\_base = 78.1
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Tested with SPEC CPU\textsuperscript{*2017} v1.0.5 on 2019-08-13 19:29:12-0400.
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