Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240M, 2.60GHz)

SPECrater®2017_int_base = 230
SPECrater®2017_int_peak = 241

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Copies

500.perlbench_r 72
520.gcc_r 72
505.mcf_r 72
520.omnetpp_r 72
523.xalancbmk_r 72
525.x264_r 72
531.deepsjeng_r 72
541.leela_r 72
548.exchange2_r 72
557.xz_r 72

SPECrater®2017_int_base (230) -- SPECrater®2017_int_peak (241)

Hardware
CPU Name: Intel Xeon Gold 6240M
Max MHz: 3900
Nominal: 2600
Enabled: 36 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Server 15
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4d released May-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: --
### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>72</td>
<td>655</td>
<td>175</td>
<td>658</td>
<td>174</td>
<td>654</td>
<td>175</td>
<td>72</td>
<td>567</td>
<td>202</td>
<td>567</td>
<td>202</td>
<td>569</td>
<td>202</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>72</td>
<td>564</td>
<td>181</td>
<td>557</td>
<td>183</td>
<td>559</td>
<td>183</td>
<td>72</td>
<td>479</td>
<td>213</td>
<td>478</td>
<td>213</td>
<td>477</td>
<td>214</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>72</td>
<td>383</td>
<td>303</td>
<td>383</td>
<td>304</td>
<td>384</td>
<td>303</td>
<td>72</td>
<td>384</td>
<td>303</td>
<td>383</td>
<td>304</td>
<td>382</td>
<td>304</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>72</td>
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<td>147</td>
<td>643</td>
<td>147</td>
<td>642</td>
<td>147</td>
<td>72</td>
<td>642</td>
<td>147</td>
<td>642</td>
<td>147</td>
<td>643</td>
<td>147</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>72</td>
<td>300</td>
<td>253</td>
<td>301</td>
<td>253</td>
<td>300</td>
<td>253</td>
<td>72</td>
<td>272</td>
<td>279</td>
<td>272</td>
<td>279</td>
<td>272</td>
<td>279</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>72</td>
<td>276</td>
<td>458</td>
<td>275</td>
<td>458</td>
<td>275</td>
<td>458</td>
<td>72</td>
<td>265</td>
<td>476</td>
<td>264</td>
<td>474</td>
<td>265</td>
<td>476</td>
</tr>
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<td>72</td>
<td>429</td>
<td>192</td>
<td>428</td>
<td>193</td>
<td>427</td>
<td>193</td>
<td>72</td>
<td>429</td>
<td>193</td>
<td>430</td>
<td>192</td>
<td>428</td>
<td>193</td>
</tr>
<tr>
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<td>72</td>
<td>644</td>
<td>185</td>
<td>645</td>
<td>185</td>
<td>649</td>
<td>184</td>
<td>72</td>
<td>647</td>
<td>184</td>
<td>640</td>
<td>186</td>
<td>645</td>
<td>185</td>
</tr>
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<td>72</td>
<td>397</td>
<td>475</td>
<td>397</td>
<td>475</td>
<td>397</td>
<td>475</td>
<td>72</td>
<td>398</td>
<td>474</td>
<td>398</td>
<td>474</td>
<td>397</td>
<td>475</td>
</tr>
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<td>72</td>
<td>515</td>
<td>151</td>
<td>514</td>
<td>151</td>
<td>514</td>
<td>151</td>
<td>72</td>
<td>514</td>
<td>151</td>
<td>514</td>
<td>151</td>
<td>515</td>
<td>151</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 230**

**SPECrate®2017_int_peak = 241**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
Memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
```
sync; echo 3>       /proc/sys/vm/drop_caches
```
Runcpu command invoked through numactl i.e.:
```
numactl --interleave=all runcpu <etc>
```
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240M, 2.60GHz)

| SPECrate®2017_int_base = 230 |
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General Notes (Continued)

is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-3c6s Tue Aug  6 16:08:49 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6240M CPU @ 2.60GHz
    2 "physical id"s (chips)
    72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
    siblings : 36
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 2
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240M CPU @ 2.60GHz
Stepping: 7

(Continued on next page)
### SPEC CPU®2017 Integer Rate Result

**Cisco Systems**  
Cisco UCS C240 M5 (Intel Xeon Gold 6240M, 2.60GHz)  

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Aug-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

#### Platform Notes (Continued)

- **CPU MHz:** 2600.000
- **CPU max MHz:** 3900.0000
- **CPU min MHz:** 1000.0000
- **BogoMIPS:** 5200.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 25344K
- **NUMA node0 CPU(s):** 0-2,5,6,9,10,14,15,36-38,41,42,45,46,50,51
- **NUMA node1 CPU(s):** 3,4,7,8,11-13,16,17,39,40,43,44,47-49,52,53
- **NUMA node2 CPU(s):** 18-20,23,24,27,28,32,33,54-56,59,60,63,64,68,69
- **NUMA node3 CPU(s):** 21,22,25,26,29-31,34,35,57,58,61,62,65-67,70,71
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pppin mba tpr_shadow vni flexpriority ept vpd fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erns invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavevc xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

```
/platform/cpuinfo cache data
  cache size : 25344 KB
```

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 5 6 9 10 14 15 36 37 38 41 42 45 46 50 51
  node 0 size: 192102 MB
  node 0 free: 191749 MB
  node 1 cpus: 3 4 7 8 11 12 13 16 17 39 40 43 44 47 48 49 52 53
  node 1 size: 193527 MB
  node 1 free: 193309 MB
  node 2 cpus: 18 19 20 23 24 27 28 32 33 54 55 56 59 60 63 64 68 69
  node 2 size: 193498 MB
  node 2 free: 193256 MB
  node 3 cpus: 21 22 25 26 29 30 31 34 35 57 58 61 62 65 66 67 70 71
  node 3 size: 193525 MB
  node 3 free: 193140 MB
  node distances:
    node 0 1 2 3
    0: 10 11 21 21
```

(Continued on next page)
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Platform Notes (Continued)

1:  11  10  21  21  
2:  21  21  10  11  
3:  21  21  11  10

From /proc/meminfo
MemTotal: 791197380 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"  
VERSION="15"  
VERSION_ID="15"  
PRETTY_NAME="SUSE Linux Enterprise Server 15"  
ID="sles"  
ID_LIKE="suse"  
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:  
Linux linux-3c6s 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)  
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected  
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization  
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 6 15:51

SPEC is set to: /home/cpu2017  
Filesystem Type Size Used Avail Use% Mounted on  
/dev/sda1 xfs 224G 20G 204G 9% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
Memory:  
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240M, 2.60GHz)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

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SPECrate®2017_int_peak = 241

CPU2017 License: 9019
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Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
[Continued on next page]
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Cisco UCS C240 M5 (Intel Xeon Gold 6240M, 2.60GHz)

SPEC CPU®2017 Integer Rate Result
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Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

(Continued on next page)
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Base Portability Flags (Continued)

502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11

C++ benchmarks (except as noted below):
icpc -m64
523.xalancbmk: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

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Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

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Peak Optimization Flags (Continued)

C++ benchmarks:
520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-ipo-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -ipo-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-ipo-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links: