## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>182</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

### CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Aug-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 6246
- **Max MHz:** 4200
- **Nominal:** 3300
- **Enabled:** 24 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 24.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Desktop 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4g released Jul-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>48</td>
<td>569</td>
<td>134</td>
<td>563</td>
<td>136</td>
<td>562</td>
<td>136</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>48</td>
<td>461</td>
<td>147</td>
<td>459</td>
<td>148</td>
<td>460</td>
<td>148</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>48</td>
<td>315</td>
<td>246</td>
<td>317</td>
<td>245</td>
<td>316</td>
<td>245</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>48</td>
<td>581</td>
<td>108</td>
<td>580</td>
<td>109</td>
<td>582</td>
<td>108</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>48</td>
<td>235</td>
<td>216</td>
<td>236</td>
<td>215</td>
<td>236</td>
<td>215</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>48</td>
<td>222</td>
<td>379</td>
<td>222</td>
<td>378</td>
<td>222</td>
<td>379</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>48</td>
<td>366</td>
<td>150</td>
<td>366</td>
<td>150</td>
<td>366</td>
<td>150</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>48</td>
<td>548</td>
<td>145</td>
<td>554</td>
<td>143</td>
<td>556</td>
<td>143</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>48</td>
<td>341</td>
<td>368</td>
<td>342</td>
<td>368</td>
<td>341</td>
<td>369</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>48</td>
<td>456</td>
<td>114</td>
<td>454</td>
<td>114</td>
<td>454</td>
<td>114</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
`sync; echo 3> /proc/sys/vm/drop_caches`

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrater®2017_int_base = 182
SPECrater®2017_int_peak = Not Run

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

    model name : Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz
    2  "physical id"s (chips)
    48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 12
    siblings : 24
    physical 0: cores 0 2 4 8 10 17 18 19 20 24 25 27
    physical 1: cores 0 2 8 9 10 17 18 19 20 25 26 27

From lscpu:
    Architecture: x86_64
    CPU op-mode(s): 32-bit, 64-bit
    Byte Order: Little Endian
    CPU(s): 48
    On-line CPU(s) list: 0-47
    Thread(s) per core: 2
    Core(s) per socket: 12
    Socket(s): 2
    NUMA node(s): 4
    Vendor ID: GenuineIntel
    CPU family: 6
    Model: 85
    Model name: Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz
    Stepping: 7
    CPU MHz: 3300.000
    CPU max MHz: 4200.0000
    CPU min MHz: 1200.0000
    BogoMIPS: 6600.00
    Virtualization: VT-x
    L1d cache: 32K
    L1i cache: 32K
    L2 cache: 1024K

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Aug-2019</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**SPEC CPU®2017 Integer Rate Result**

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>182</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

L3 cache: 25344K
NUMA node0 CPU(s): 0,1,3,5,9,10,24,25,27,29,33,34
NUMA node1 CPU(s): 2,4,6-8,11,26,28,30-32,35
NUMA node2 CPU(s): 12-15,17,21,36-39,41,45
NUMA node3 CPU(s): 16,18-20,22,23,40,42-44,46,47
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl svm smx est tm2 ssse3
sdbg fma cx16 xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
eb cat_tsa cpuid tsc_adjust bmi1 hle avx2 smep bmi2 ibrms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsave xsavec xgetbv1 xsaves cqm_llc cqm_occupy_llc cqm_mbb_total cqm_mbb_local
ibpb ibrs ibrs ibrs dtlbmt ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pkup
ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
cache size : 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 3 5 9 10 24 25 27 29 33 34
node 0 size: 192063 MB
node 0 free: 191748 MB
node 1 cpus: 2 4 6 7 8 11 26 28 30 31 32 35
node 1 size: 193523 MB
node 1 free: 193259 MB
node 2 cpus: 12 13 14 15 17 21 36 37 38 39 41 45
node 2 size: 193523 MB
node 2 free: 193282 MB
node 3 cpus: 16 18 19 20 22 23 40 42 43 44 46 47
node 3 size: 193520 MB
node 3 free: 193262 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791173828 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrate®2017_int_base = 182
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLED"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Desktop 15"
    ID="sled"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sled:15"

uname -a:
  Linux linux-56kd 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 7 12:44

SPEC is set to: /home/cpu2017
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda1 xfs 894G 22G 872G 3% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.4.0.4g.0.0712190011 07/12/2019
  Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

================================================================================
| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) |
| 525.x264_r(base) 557.xz_r(base) |
================================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECRate®2017_int_base = 182
SPECRate®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-------------------------------
C++ | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
     | 541.leela_r(base)
-------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-------------------------------
Fortran | 548.exchange2_r(base)
-------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation
C benchmarks:
         icc -m64 -std=c11
C++ benchmarks:
         icpc -m64
Fortran benchmarks:
         ifort -m64

Base Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrate®2017_int_base = 182
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Portability Flags (Continued)

557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links: