Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5220, 2.20GHz)

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base = 121</th>
</tr>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>36</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>36</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>36</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>36</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>36</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>36</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>36</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>36</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>36</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>36</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 5220
- **Max MHz:** 3900
- **Nominal:** 2200
- **Enabled:** 36 cores, 2 chips
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I+ 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 24.75 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
- **Storage:** 1 x 240 GB M.2 SATA SSD
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux;
  Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_fp_base = 121
SPECspeed®2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>84.3</td>
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<td>115</td>
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<tr>
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<td>136</td>
<td>116</td>
<td>142</td>
<td>111</td>
<td>135</td>
<td>116</td>
</tr>
</tbody>
</table>

SPECspeed®2017_fp_base = 121
SPECspeed®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

(Continued on next page)
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<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>121</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
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</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: Mar-2019

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-bo6o Sun Aug 18 16:52:13 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores: 18
  - siblings: 18
  - physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  - physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 36
- On-line CPU(s) list: 0-35
- Thread(s) per core: 1
- Core(s) per socket: 18
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz
- Stepping: 6
- CPU MHz: 2200.000
- CPU max MHz: 3900.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 4400.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 25344K

(Continued on next page)
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SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

SPECspeed®2017 fp_base = 121
SPECspeed®2017 fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: Mar-2019

Platform Notes (Continued)

NUMA node0 CPU(s): 0-17
NUMA node1 CPU(s): 18-35
Flags: fpu vme de pse tsc msr pae mce cx8 apa sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref perf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
ebh cat_13 cdp_13 invpcid_single intel_ppin mba tpr_shadow vmmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospe avx512_vnni arch_capabilities ssbd

/cache data

```
 From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
 available: 2 nodes (0-1)
 node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
 node 0 size: 385428 MB
 node 0 free: 383068 MB
 node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
 node 1 size: 387045 MB
 node 1 free: 383770 MB
 node distances:
 node 0 1
 0: 10 21
 1: 21 10
```

From /proc/meminfo
```
MemTotal: 791013368 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

From /etc/*release* /etc/*version*
oo-release:
```
 NAME="SLES"
 VERSION="15"
 VERSION_ID="15"
 PRETTY_NAME="SUSE Linux Enterprise Server 15"
 ID="sles"
 ID_LIKE="suse"
 ANSI_COLOR="0;32"
 CPE_NAME="cpe:/o:suse:sles:15"
```
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

uname -a:
    Linux linux-bo60 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 18 15:43

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb1 btrfs 224G 17G 207G 8% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
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Cisco Systems

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| SPECspeed®2017_fp_base = | 121 |
| SPECspeed®2017_fp_peak = | Not Run |

| CPU2017 License: | 9019 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |
| Test Date: | Aug-2019 |
| Hardware Availability: | Apr-2019 |
| Software Availability: | Mar-2019 |

### Compiler Version Notes (Continued)

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<tr>
<th>Fortran</th>
<th>603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)</th>
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<tbody>
<tr>
<td>Intel(R) Fortran</td>
<td>Intel(R) 64 Compiler for applications running on Intel(R)</td>
</tr>
<tr>
<td>64</td>
<td>64, Version 19.0.1.144 Build 20181018</td>
</tr>
<tr>
<td>Copyright (C)</td>
<td>1985-2018 Intel Corporation. All rights reserved.</td>
</tr>
</tbody>
</table>

```
Base Compiler Invocation

C benchmarks:
   icc -m64 -std=c11

Fortran benchmarks:
   ifort -m64

Benchmarks using both Fortran and C:
   ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
   icpc -m64 icc -m64 -std=c11 ifort -m64
```

### Base Portability Flags

- 603.bwaves_s: -DSPEC_LP64
- 607.cactuBSSN_s: -DSPEC_LP64
- 619.lbm_s: -DSPEC_LP64
- 621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 638.imagick_s: -DSPEC_LP64
- 644.nab_s: -DSPEC_LP64

(Continued on next page)
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Base Portability Flags (Continued)

649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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