**Cisco Systems**
Cisco UCS B200 M5 (Intel Xeon Gold 6230, 2.10GHz)

**SPEC CPU<sup>®</sup>2017 Floating Point Rate Result**

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>206</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**Copyright 2017-2019 Standard Performance Evaluation Corporation**

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

**Hardware**

<table>
<thead>
<tr>
<th>CPU Name:</th>
<th>Intel Xeon Gold 6230</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max MHz:</td>
<td>3900</td>
</tr>
<tr>
<td>Nominal:</td>
<td>2100</td>
</tr>
<tr>
<td>Enabled:</td>
<td>40 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1,2 chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3:</td>
<td>27.5 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Memory:</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)</td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 1.9 TB SSD SAS</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
</tbody>
</table>

**Software**

<table>
<thead>
<tr>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux</td>
</tr>
<tr>
<td>Parallel:</td>
<td>No</td>
</tr>
<tr>
<td>Firmware:</td>
<td>Version 4.0.4b released Apr-2019</td>
</tr>
<tr>
<td>File System:</td>
<td>xfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Power Management:</td>
<td>--</td>
</tr>
</tbody>
</table>

---

Copies

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base (206)</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r 80</td>
</tr>
<tr>
<td>507.caCTuBSSN_r 80</td>
</tr>
<tr>
<td>508.namd_r 80</td>
</tr>
<tr>
<td>510.parest_r 80</td>
</tr>
<tr>
<td>511.povray_r 80</td>
</tr>
<tr>
<td>519.lbm_r 80</td>
</tr>
<tr>
<td>521.wrf_r 80</td>
</tr>
<tr>
<td>526.blender_r 80</td>
</tr>
<tr>
<td>527.cam4_r 80</td>
</tr>
<tr>
<td>538.imagick_r 80</td>
</tr>
<tr>
<td>544.nab_r 80</td>
</tr>
<tr>
<td>549.fotonik3d_r 80</td>
</tr>
<tr>
<td>554.roms_r 80</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6230, 2.10GHz)

SPECrate®2017_fp_base = 206
SPECrate®2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>80</td>
<td>1601</td>
<td>501</td>
<td>1602</td>
<td>501</td>
<td>1601</td>
<td>501</td>
<td></td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>80</td>
<td>617</td>
<td>164</td>
<td>616</td>
<td>164</td>
<td>617</td>
<td>164</td>
<td></td>
<td></td>
</tr>
<tr>
<td>508.namd_r</td>
<td>80</td>
<td>477</td>
<td>159</td>
<td>477</td>
<td>159</td>
<td>479</td>
<td>159</td>
<td></td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td>80</td>
<td>1808</td>
<td>116</td>
<td>1806</td>
<td>116</td>
<td>1804</td>
<td>116</td>
<td></td>
<td></td>
</tr>
<tr>
<td>511.povray_r</td>
<td>80</td>
<td>806</td>
<td>232</td>
<td>806</td>
<td>232</td>
<td>805</td>
<td>232</td>
<td></td>
<td></td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>80</td>
<td>693</td>
<td>122</td>
<td>692</td>
<td>122</td>
<td>692</td>
<td>122</td>
<td></td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>80</td>
<td>847</td>
<td>212</td>
<td>847</td>
<td>212</td>
<td>838</td>
<td>214</td>
<td></td>
<td></td>
</tr>
<tr>
<td>526.blender_r</td>
<td>80</td>
<td>564</td>
<td>216</td>
<td>565</td>
<td>216</td>
<td>565</td>
<td>216</td>
<td></td>
<td></td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>80</td>
<td>596</td>
<td>235</td>
<td>598</td>
<td>234</td>
<td>598</td>
<td>234</td>
<td></td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>80</td>
<td>411</td>
<td>484</td>
<td>416</td>
<td>478</td>
<td>413</td>
<td>482</td>
<td></td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td>80</td>
<td>392</td>
<td>343</td>
<td>390</td>
<td>346</td>
<td>394</td>
<td>342</td>
<td></td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>80</td>
<td>1905</td>
<td>164</td>
<td>1906</td>
<td>164</td>
<td>1906</td>
<td>164</td>
<td></td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>80</td>
<td>1304</td>
<td>97.5</td>
<td>1308</td>
<td>97.2</td>
<td>1305</td>
<td>97.4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6230, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrates

SPECrate®2017_fp_base = 206
SPECrate®2017_fp_peak = Not Run

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-3xnd Sat Aug 17 17:27:45 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6230 CPU @ 2.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85

(Continued on next page)
### Platform Notes (Continued)

Model name: Intel(R) Xeon(R) Gold 6230 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000
CPU max MHz: 3900.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56
NUMA node1 CPU(s): 3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59
NUMA node2 CPU(s): 20-22,25,26,30-32,35,36,60-62,65,66,70-72,74,75,76
NUMA node3 CPU(s): 23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmrperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdmb fma cx16 xtrm pcdc pclid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdpl3 invpcid_single intel_pinn mba tpr_shadow vmni flexpriority ept
vpid fsgsbase tsc_adjust bni1 hle avx2 smep bmi2 emms invpcid rtm cmpx mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local
ibpb ibrs stibp dtimer ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

`/proc/cpuinfo` cache data
    cache size : 28160 KB

From `numactl --hardware` WARNING: a numactl 'node' might or might not correspond to a
physical chip.
    available: 4 nodes (0-3)
    node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
    node 0 size: 192090 MB
    node 0 free: 184316 MB
    node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
    node 1 size: 193521 MB
    node 1 free: 188856 MB
    node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
    node 2 size: 193521 MB
    node 2 free: 189021 MB
    node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
    node 3 size: 193490 MB
    node 3 free: 189053 MB
    node distances:

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6230, 2.10GHz)

SPECrate®2017_fp_base = 206
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

```
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10
```

From /proc/meminfo
```
MemTotal: 791167664 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

From /etc/*release* /etc/*version*
```
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

uname -a:
```
Linux linux-3xnd 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

run-level 3 Aug 17 11:40

SPEC is set to: /home/cpu2017
```
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb4 xfs 100G 28G 73G 28% /home
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
```
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934
```

(End of data from sysinfo program)

Compiler Version Notes

```
C | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6230, 2.10GHz)  

SPECraten®2017_fp_base = 206  
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CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Test Date: Aug-2019  
Tested by: Cisco Systems  
Hardware Availability: Apr-2019  
Software Availability: May-2019

Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

==============================================================================
C++  
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------
C++, C  
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------
C++, C, Fortran  
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------
Fortran  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems  
Cisco UCS B200 M5 (Intel Xeon Gold 6230, 2.10GHz)  

SPECraten®2017_fp_base = 206  
SPECraten®2017_fp_peak = Not Run  

Compiler Version Notes (Continued)  
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)  
---  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
---  

Base Compiler Invocation  
C benchmarks:  
icc -m64 -std=c11  

C++ benchmarks:  
icpc -m64  

Fortran benchmarks:  
ifort -m64  

Benchmarks using both Fortran and C:  
ifort -m64 icc -m64 -std=c11  

Benchmarks using both C and C++:  
icpc -m64 icc -m64 -std=c11  

Benchmarks using Fortran, C, and C++:  
icpc -m64 icc -m64 -std=c11 ifort -m64  

Base Portability Flags  
503.bwaves_r: -DSPEC_LP64  
507.cactuBSSN_r: -DSPEC_LP64  
508.namd_r: -DSPEC_LP64  
510.parest_r: -DSPEC_LP64  
511.povray_r: -DSPEC_LP64  
519.lbm_r: -DSPEC_LP64  
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian  
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char  
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG  
538.imagick_r: -DSPEC_LP64  

(Continued on next page)
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SPECrater®2017_fp_base = 206
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Base Portability Flags (Continued)

544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6230, 2.10GHz)

| SPECrate®2017_fp_base = 206 |
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-08-17 20:27:44-0400.
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