## SPEC CPU®2017 Integer Speed Result

### Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6230, 2.10GHz)

<table>
<thead>
<tr>
<th>Threads</th>
<th>0</th>
<th>1.00</th>
<th>2.00</th>
<th>3.00</th>
<th>4.00</th>
<th>5.00</th>
<th>6.00</th>
<th>7.00</th>
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<th>10.0</th>
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<th>12.0</th>
<th>13.0</th>
<th>14.0</th>
<th>15.0</th>
<th>16.0</th>
<th>17.0</th>
<th>18.0</th>
<th>19.0</th>
<th>20.0</th>
<th>21.0</th>
<th>22.0</th>
<th>23.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>112</td>
<td>6.76</td>
<td></td>
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<td>112</td>
<td>9.83</td>
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<tr>
<td>605.mcf_s</td>
<td>112</td>
<td>12.6</td>
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<td></td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>112</td>
<td>8.16</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>112</td>
<td>12.5</td>
<td></td>
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<tr>
<td>625.x264_s</td>
<td>112</td>
<td>14.5</td>
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<tr>
<td>631.deepsjeng_s</td>
<td>112</td>
<td>5.44</td>
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<tr>
<td>641.leela_s</td>
<td>112</td>
<td>4.78</td>
<td></td>
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</tr>
<tr>
<td>648.exchange2_s</td>
<td>112</td>
<td>14.1</td>
<td></td>
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<tr>
<td>657.xz_s</td>
<td>112</td>
<td>22.5</td>
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**SPECspeed®2017_int_base** = 10.0

**SPECspeed®2017_int_peak** = Not Run

### Hardware

- **CPU Name:** Intel Xeon Gold 6230
- **Max MHz:** 3900
- **Nominal:** 2100
- **Enabled:** 40 cores, 2 chips
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 27.5 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6230, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECSPEED®2017_int_base = 10.0
SPECSPEED®2017_int_peak = Not Run

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>perlbench_s</td>
<td>112</td>
<td>262</td>
<td>6.76</td>
<td>261</td>
<td>6.79</td>
<td>263</td>
<td>6.76</td>
</tr>
<tr>
<td>gcc_s</td>
<td>112</td>
<td>405</td>
<td>9.83</td>
<td>407</td>
<td>9.79</td>
<td>405</td>
<td>9.83</td>
</tr>
<tr>
<td>mcf_s</td>
<td>112</td>
<td>376</td>
<td>12.6</td>
<td>375</td>
<td>12.6</td>
<td>376</td>
<td>12.6</td>
</tr>
<tr>
<td>omnetpp_s</td>
<td>112</td>
<td>194</td>
<td>8.39</td>
<td>200</td>
<td>8.16</td>
<td>206</td>
<td>7.90</td>
</tr>
<tr>
<td>xalancbmk_s</td>
<td>112</td>
<td>114</td>
<td>12.5</td>
<td>113</td>
<td>12.5</td>
<td>114</td>
<td>12.5</td>
</tr>
<tr>
<td>x264_s</td>
<td>112</td>
<td>122</td>
<td>14.5</td>
<td>122</td>
<td>14.5</td>
<td>121</td>
<td>14.5</td>
</tr>
<tr>
<td>deepsjeng_s</td>
<td>112</td>
<td>264</td>
<td>5.44</td>
<td>263</td>
<td>5.45</td>
<td>263</td>
<td>5.44</td>
</tr>
<tr>
<td>leela_s</td>
<td>112</td>
<td>357</td>
<td>4.78</td>
<td>357</td>
<td>4.78</td>
<td>357</td>
<td>4.78</td>
</tr>
<tr>
<td>exchange2_s</td>
<td>112</td>
<td>209</td>
<td>14.1</td>
<td>209</td>
<td>14.1</td>
<td>209</td>
<td>14.1</td>
</tr>
<tr>
<td>xz_s</td>
<td>112</td>
<td>274</td>
<td>22.6</td>
<td>275</td>
<td>22.5</td>
<td>275</td>
<td>22.5</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>> /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls

(Continued on next page)
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Test Date: Aug-2019
Hardware Availability: Apr-2019
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Platform Notes (Continued)

SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618b091c0f
running on linux-3xnd Sun Aug 18 11:03:22 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6230 CPU @ 2.10GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 1
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6230 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000
CPU max MHz: 3900.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-19

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

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Cisco UCS B200 M5 (Intel Xeon Gold 6230, 2.10GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: May-2019

Platform Notes (Continued)

NUMA node1 CPU(s): 20-39
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmrperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sbeg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt

tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cpd_13 invpcid_single intel_pdm mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ertz invpcei rtm cqm mpx rdte_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local
ibpb ibrs stibp dtherm ida pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size: 28160 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
  node 0 size: 385616 MB
  node 0 free: 384113 MB
  node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
  node 1 size: 387015 MB
  node 1 free: 383372 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 791175692 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

(Continued on next page)
**Platform Notes (Continued)**

uname -a:
   Linux linux-3xnd 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 18 06:27

SPEC is set to: /home/cpu2017

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
   24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

**Compiler Version Notes**

```
C
  600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
  625.x264_s(base) 657.xz_s(base)
```

```Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

```
C++
  620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
  641.leela_s(base)
```

```Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

```
Fortran
  648.exchange2_s(base)
```

```Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
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Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600 perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602 gcc_s: -DSPEC_LP64
605 mcf_s: -DSPEC_LP64
620 omnetpp_s: -DSPEC_LP64
623 xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625 x264_s: -DSPEC_LP64
631 deepsjeng_s: -DSPEC_LP64
641 leela_s: -DSPEC_LP64
648 exchange2_s: -DSPEC_LP64
657 xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6230, 2.10GHz)  

**Base Optimization Flags (Continued)**

Fortran benchmarks (continued):
- nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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