# SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Platinum 8260, 2.40GHz)  

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td></td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td></td>
</tr>
<tr>
<td>Test Date:</td>
<td>Aug-2019</td>
<td></td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
<td></td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>277</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

## Hardware

- **CPU Name:** Intel Xeon Platinum 8260  
- **Max MHz:** 3900  
- **Nominal:** 2400  
- **Enabled:** 48 cores, 2 chips, 2 threads/core  
- **Orderable:** 1, 2 chip(s)  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 35.75 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
- **Storage:** 1 x 960 GB SATA M.2 SSD  
- **Other:** None  

## Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
  4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.0.4b released Apr-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** None  
- **Power Management:** --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8260, 2.40GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
<td>730</td>
<td>209</td>
<td>729</td>
<td>210</td>
<td>727</td>
<td>210</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>96</td>
<td>608</td>
<td>223</td>
<td>622</td>
<td>223</td>
<td>605</td>
<td>225</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>96</td>
<td>434</td>
<td>357</td>
<td>435</td>
<td>357</td>
<td>435</td>
<td>357</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>96</td>
<td>712</td>
<td>177</td>
<td>713</td>
<td>177</td>
<td>713</td>
<td>177</td>
</tr>
<tr>
<td>523.xalanbmkm_r</td>
<td>96</td>
<td>339</td>
<td>299</td>
<td>340</td>
<td>299</td>
<td>338</td>
<td>300</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>96</td>
<td>298</td>
<td>565</td>
<td>298</td>
<td>564</td>
<td>299</td>
<td>562</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>96</td>
<td>479</td>
<td>230</td>
<td>478</td>
<td>230</td>
<td>479</td>
<td>230</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>96</td>
<td>731</td>
<td>217</td>
<td>717</td>
<td>222</td>
<td>717</td>
<td>222</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>96</td>
<td>448</td>
<td>561</td>
<td>449</td>
<td>560</td>
<td>449</td>
<td>560</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>96</td>
<td>562</td>
<td>185</td>
<td>564</td>
<td>184</td>
<td>563</td>
<td>184</td>
</tr>
</tbody>
</table>

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8260, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>277</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-3xnd Thu Aug 22 15:12:42 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8260 CPU @ 2.40GHz
 2 "physical id"s (chips)
 96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8260 CPU @ 2.40GHz
Stepping: 6
CPU MHz: 2400.000

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8260, 2.40GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: May-2019

SPECrate®2017_int_base = 277
SPECrate®2017_int_peak = Not Run

Platform Notes (Continued)

CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-3,7-9,13-15,19,20,48-51,55-57,61-63,67,68
NUMA node1 CPU(s): 4-6,10-12,16-18,21-23,52-54,58-60,64-66,69-71
NUMA node2 CPU(s): 24-27,31,32,36-38,42-44,72-75,79,80,84-86,90-92
NUMA node3 CPU(s): 28-30,33-35,39-41,45,47,76-78,81-83,87-89,93-95
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq intel_pni mba tpr_shadow vnni flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ermi invpcid rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves xsaveopt xsaveprec xsavecpuid xcx xmx vmmware smt x2apic movbe popcnt

tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_pplin mba tpr_shadow vnni flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqmp mxp rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves xsaveopt xsaveprec xsavecpuid xcx xmx vmmware smt x2apic movbe popcnt

tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_pplin mba tpr_shadow vnni flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqmp mxp rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves xsaveopt xsaveprec xsavecpuid xcx xmx vmmware smt x2apic movbe popcnt

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

number of nodes: 4
node 0 cpus: 0 1 2 3 7 8 9 13 14 15 19 20 48 49 50 51 55 56 57 61 62 63 67 68
node 0 size: 192090 MB
node 0 free: 191752 MB
node 1 cpus: 4 5 6 10 11 12 16 17 18 21 22 23 52 53 54 58 59 60 64 65 66 69 70 71
node 1 size: 193521 MB
node 1 free: 193045 MB
node 2 cpus: 24 25 26 27 31 32 36 37 38 42 43 44 72 73 74 75 79 80 84 85 86 90 91 92
node 2 size: 193521 MB
node 2 free: 193265 MB
node 3 cpus: 28 29 30 33 34 35 39 40 41 45 46 47 76 77 78 81 82 83 87 88 89 93 94 95
node 3 size: 193489 MB
node 3 free: 193252 MB

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8260, 2.40GHz)

**SPECrate®2017_int_base = 277**
**SPECrate®2017_int_peak = Not Run**

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Aug-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
</tbody>
</table>

---

**Platform Notes (Continued)**

```
2:  21  21  10  11
3:  21  21  11  10
```

From `/proc/meminfo`

- MemTotal: 791164588 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release* /etc/*version*`

```bash
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
Linux linux-3xnd 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

```
runtime 3 Aug 22 14:45
SPEC is set to: /home/cpu2017
```

```
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb4 xfs 100G 13G 88G 13% /home
```

Additional information from `dmidecode` follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019

Memory:
- 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

---

**Compiler Version Notes**

```
==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
| 525.x264_r(base) 557.xz_r(base)
==============================================================================
```

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8260, 2.40GHz)

SPECratre®2017_int_base = 277
SPECratre®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
| C++                      | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) 541.leela_r(base) |
------------------------------------------------------------------------------
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416                                     |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved.        |
------------------------------------------------------------------------------
| Fortran                  | 548.exchange2_r(base) |
------------------------------------------------------------------------------
| Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) |
| 64, Version 19.0.4.227 Build 20190416                                  |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved.        |
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8260, 2.40GHz)

**SPECrate®2017_int_base = 277**

**SPECrate®2017_int_peak = Not Run**

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date</td>
<td>Aug-2019</td>
</tr>
<tr>
<td>Hardware Availability</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**Base Portability Flags (Continued)**

557.xz_r: -DSPEC_LP64

**Base Optimization Flags**

**C benchmarks:**
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc`

**C++ benchmarks:**
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc`

**Fortran benchmarks:**
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc`

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-08-22 18:12:42-0400.
Report generated on 2020-07-02 18:04:06 by CPU2017 PDF formatter v6255.
Originally published on 2019-09-19.