Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8280, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base =</th>
<th>276</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak =</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019  Test Date: Aug-2019
Test Sponsor: Cisco Systems  Hardware Availability: Apr-2019
Tested by: Cisco Systems  Software Availability: May-2019

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Platinum 8280  OS: SUSE Linux Enterprise Server 15 (x86_64)</td>
<td></td>
</tr>
<tr>
<td>Max MHz: 4000  4.12.14-23-default</td>
<td></td>
</tr>
<tr>
<td>Nominal: 2700  Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux</td>
<td></td>
</tr>
<tr>
<td>Enabled: 56 cores, 2 chips, 2 threads/core  Parallel: No</td>
<td></td>
</tr>
<tr>
<td>Orderable: 1,2 Chips  Firmware: Version 4.0.4b released Apr-2019</td>
<td></td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 32 KB D on chip per core  System State: Run level 3 (multi-user)</td>
<td></td>
</tr>
<tr>
<td>L2: 1 MB I+D on chip per core  Base Pointers: 64-bit</td>
<td></td>
</tr>
<tr>
<td>L3: 38.5 MB I+D on chip per chip  Peak Pointers: Not Applicable</td>
<td></td>
</tr>
<tr>
<td>Other: None  Other: None</td>
<td></td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  Power Management: --</td>
<td></td>
</tr>
<tr>
<td>Storage: 1 x 240 GB M.2 SATA SSD</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Software Availability: May-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copies</td>
</tr>
<tr>
<td>---------------------</td>
</tr>
<tr>
<td>503.bwaves_r</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
</tr>
<tr>
<td>508.namd_r</td>
</tr>
<tr>
<td>510.parest_r</td>
</tr>
<tr>
<td>511.povray_r</td>
</tr>
<tr>
<td>519.lbm_r</td>
</tr>
<tr>
<td>521.wrf_r</td>
</tr>
<tr>
<td>526.blender_r</td>
</tr>
<tr>
<td>527.cam4_r</td>
</tr>
<tr>
<td>538.imagick_r</td>
</tr>
<tr>
<td>544.nab_r</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
</tr>
<tr>
<td>554.roms_r</td>
</tr>
</tbody>
</table>
### Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8280, 2.70GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>112</td>
<td>2092</td>
<td>537</td>
<td>2091</td>
<td>537</td>
<td>2091</td>
<td>537</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>112</td>
<td>580</td>
<td>245</td>
<td>580</td>
<td>244</td>
<td>580</td>
<td>245</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>508.namd_r</td>
<td>112</td>
<td>415</td>
<td>256</td>
<td>415</td>
<td>256</td>
<td>415</td>
<td>256</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td>112</td>
<td>2188</td>
<td>134</td>
<td>2188</td>
<td>134</td>
<td>2183</td>
<td>134</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>511.povray_r</td>
<td>112</td>
<td>699</td>
<td>374</td>
<td>702</td>
<td>373</td>
<td>701</td>
<td>373</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>112</td>
<td>901</td>
<td>131</td>
<td>901</td>
<td>131</td>
<td>901</td>
<td>131</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>112</td>
<td>1044</td>
<td>240</td>
<td>1054</td>
<td>238</td>
<td>1046</td>
<td>240</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>526.blender_r</td>
<td>112</td>
<td>491</td>
<td>347</td>
<td>491</td>
<td>347</td>
<td>491</td>
<td>347</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>112</td>
<td>536</td>
<td>365</td>
<td>536</td>
<td>365</td>
<td>538</td>
<td>364</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>112</td>
<td>355</td>
<td>784</td>
<td>356</td>
<td>783</td>
<td>355</td>
<td>784</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td>112</td>
<td>333</td>
<td>566</td>
<td>335</td>
<td>562</td>
<td>333</td>
<td>565</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>112</td>
<td>2524</td>
<td>173</td>
<td>2522</td>
<td>173</td>
<td>2524</td>
<td>173</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>112</td>
<td>1701</td>
<td>105</td>
<td>1693</td>
<td>105</td>
<td>1706</td>
<td>104</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 276**

**SPECrate®2017_fp_peak = Not Run**

### Results Table

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

sync; echo 3 > /proc/sys/vm/drop_caches

runcpu command invoked through numactl i.e.:

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8280, 2.70GHz)

SPECrate®2017_fp_base = 276
SPECrate®2017_fp_peak = Not Run

General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-pmqx Thu Aug 15 15:04:54 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Platinum 8280 CPU @ 2.70GHz
   2 "physical id"s (chips)
   112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 28
siblings: 56
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 112
On-line CPU(s) list: 0-111
Thread(s) per core: 2
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 4

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**

**Cisco UCS B200 M5 (Intel Xeon Platinum 8280, 2.70GHz)**

<table>
<thead>
<tr>
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<tr>
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<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Aug-2019</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**SPECrater®2017_fp_base = 276**

**SPECrater®2017_fp_peak = Not Run**

### Platfrom Notes (Continued)

- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Platinum 8280 CPU @ 2.70GHz
- Stepping: 7
- CPU MHz: 2700.000
- CPU max MHz: 4000.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 5400.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 39424K
- NUMA node0 CPU(s): 0-3,7-9,14-17,21-23,56-59,63-73,77-79
- NUMA node1 CPU(s): 4-6,10-13,18-20,24-27,60-62,66-69,74-76,80-83
- NUMA node2 CPU(s): 28-31,35-37,42-45,49-51,84-87,91-93,98-101,105-107
- NUMA node3 CPU(s): 32-34,38-41,46-48,52-55,88-90,94-97,102-104,108-111
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmpcr tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrnr pdcm pclid dca SSE4_1 SSE4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebpx cat_l3 cdp_l3 invpcid_single intel_pmm mba tpr_shadow sknmi flexpriority ept vpid fsbgbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsave xsvme xsavec xsaveopt xgetbv xsavec xsaveopt cqm_llc cqm_occupy llc cqm_mbm_total cqm_mbm_local ibpb ibrs ibrs tdir dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req kpu osprk avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

- available: 4 nodes (0-3)
- node 0 cpus: 0 1 2 3 7 8 9 14 15 16 17 21 22 23 56 57 58 59 63 64 65 70 71 72 73 77 78 79
- node 0 size: 192089 MB
- node 0 free: 184239 MB
- node 1 cpus: 4 5 6 10 11 12 13 18 19 20 24 25 26 27 60 61 62 66 67 68 69 74 75 76 80 81 82 83
- node 1 size: 193520 MB
- node 1 free: 187582 MB
- node 2 cpus: 28 29 30 31 35 36 37 42 43 44 45 49 50 51 84 85 86 87 91 92 93 98 99 100 101 105 106 107

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8280, 2.70GHz)

SPECrate®2017_fp_base = 276
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

node 2 size: 193520 MB
node 2 free: 187663 MB
node 3 cpus: 32 33 34 38 40 41 46 47 48 52 54 55 58 89 90 94 95 96 97 102 103 104
node 3 size: 193488 MB
node 3 free: 187560 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791161488 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-pmqx 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Aug 15 10:01

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb4 btrfs 169G 36G 133G 22% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8280, 2.70GHz)

Platform Notes (Continued)

(End of data from sysinfo program)

Compiler Version Notes

C

519.libm_r(base) 538.imagick_r(base) 544.nab_r(base)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

C++

508.namd_r(base) 510.parest_r(base)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

C++, C

511.povray_r(base) 526.blender_r(base)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

C++, C, Fortran

507.cactuBSSN_r(base)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8280, 2.70GHz)  
SPECrat©2017_fp_base = 276  
SPECrat©2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
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</tr>
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</tr>
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<tr>
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</tr>
</tbody>
</table>

**Compiler Version Notes (Continued)**

<table>
<thead>
<tr>
<th>Compiler</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fortran</td>
<td>503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)</td>
</tr>
<tr>
<td></td>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018</td>
</tr>
<tr>
<td></td>
<td>Copyright (C) 1985-2018 Intel Corporation. All rights reserved.</td>
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</tbody>
</table>

**Base Compiler Invocation**

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

**Base Portability Flags**

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8280, 2.70GHz)

SPECrate®2017_fp_base = 276
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Portability Flags (Continued)

510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at
### SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**  
Cisco UCS B200 M5 (Intel Xeon Platinum 8280, 2.70GHz)  

<table>
<thead>
<tr>
<th>Specification</th>
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</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_base</td>
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<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019  

You can also download the XML flags sources by saving the following links:  

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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