**SPEC CPU®2017 Integer Speed Result**

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Gold 5222, 3.80GHz)

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Aug-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

| SPECspeed®2017_int_base = 9.35 |
| SPECspeed®2017_int_peak = Not Run |

| CPU2017 License: | 9019 |
| Test Date: | Aug-2019 |
| Software Availability: | May-2019 |
| Hardware Availability: | Apr-2019 |

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_int_base (9.35)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
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<tr>
<td>4</td>
<td></td>
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<tr>
<td>5</td>
<td></td>
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<tr>
<td>6</td>
<td></td>
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<tr>
<td>7</td>
<td></td>
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<tr>
<td>8</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
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<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 5222
- **Max MHz:** 3900
- **Nominal:** 3800
- **Enabled:** 8 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 16.5 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2934)
- **Storage:** 1 x 600G SAS 10K RPM
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --
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Test Sponsor: Cisco Systems
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SPECspeed®2017_int_base = 9.35
SPECspeed®2017_int_peak = Not Run

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>8</td>
<td>264</td>
<td>6.72</td>
<td>264</td>
<td>6.72</td>
<td>263</td>
<td>6.74</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>8</td>
<td>429</td>
<td>9.29</td>
<td>427</td>
<td>9.33</td>
<td>431</td>
<td>9.24</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>8</td>
<td>380</td>
<td>12.4</td>
<td>379</td>
<td>12.4</td>
<td>380</td>
<td>12.4</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>8</td>
<td>263</td>
<td>6.19</td>
<td>262</td>
<td>6.22</td>
<td>264</td>
<td>6.17</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>8</td>
<td>115</td>
<td>12.3</td>
<td>115</td>
<td>12.3</td>
<td>115</td>
<td>12.3</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>8</td>
<td>124</td>
<td>14.2</td>
<td>124</td>
<td>14.2</td>
<td>124</td>
<td>14.2</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>8</td>
<td>263</td>
<td>5.45</td>
<td>263</td>
<td>5.45</td>
<td>263</td>
<td>5.44</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>8</td>
<td>358</td>
<td>4.77</td>
<td>357</td>
<td>4.78</td>
<td>358</td>
<td>4.77</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>8</td>
<td>176</td>
<td>16.7</td>
<td>176</td>
<td>16.7</td>
<td>176</td>
<td>16.7</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>8</td>
<td>442</td>
<td>14.0</td>
<td>442</td>
<td>14.0</td>
<td>442</td>
<td>14.0</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
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<td>Not Run</td>
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</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-k1c6 Sat Aug 24 16:28:50 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5222 CPU @ 3.80GHz
  2 "physical id"s (chips)
  8 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 4
physical 0: cores 5 8 9 13
physical 1: cores 2 5 9 13

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 8
On-line CPU(s) list: 0-7
Thread(s) per core: 1
Core(s) per socket: 4
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5222 CPU @ 3.80GHz
Stepping: 6
CPU MHz: 3800.000
CPU max MHz: 3900.0000
CPU min MHz: 1200.0000
BogoMIPS: 7600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K

(Continued on next page)
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Platform Notes (Continued)

L3 cache: 16896K
NUMA node0 CPU(s): 0-3
NUMA node1 CPU(s): 4-7
Flags:

fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
eb cat_l3 cdp_l3 invpcid_single intel_pippin mba tpr_shadow vnumi flexpriority ept
vpid fsgsbase tsc_adjust bm1 hle avx2 smep bmi2 ermv invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsavesopt xsavec xgetbv1 xsaveopt xsave cqm_llc cqm_occup_llc cqm_mmb_total cqm_mmb_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
cache size : 16896 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3
node 0 size: 385460 MB
node 0 free: 380995 MB
node 1 cpus: 4 5 6 7
node 1 size: 387018 MB
node 1 free: 386537 MB
node distances:

node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 791018772 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"

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Platform Notes (Continued)

CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
   Linux linux-k1c6 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
   x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 24 13:54

SPEC is set to: /home/cpu2017

Filesystem   Type   Size  Used Avail Use% Mounted on
/dev/sdc2     btrfs  557G   18G  539G   4% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
   Memory:
      24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

C
-----------------------------------
   600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
   625.x264_s(base) 657.xz_s(base)

-----------------------------------

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++
-----------------------------------
   620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
   641.leea_s(base)

-----------------------------------

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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Fortran
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)

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**Compiler Version Notes (Continued)**

64, Version 19.0.4.227 Build 20190416
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Base Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

Base Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
```

Base Optimization Flags

```
C benchmarks:
-Wl, -z, muldefs -xcORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -gopenmp -DSPEC_OPENMP
-\L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl, -z, muldefs -xcORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-\L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

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Base Optimization Flags (Continued)

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout=trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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