## SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Platinum 8270, 2.70GHz)

**SPECspeed®2017_fp_base = 151**

**SPECspeed®2017_fp_peak = Not Run**

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base (151)</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>52</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>52</td>
</tr>
<tr>
<td>619.ibm_s</td>
<td>52</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>52</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>52</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>52</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>52</td>
</tr>
<tr>
<td>641.nab_s</td>
<td>52</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>52</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>52</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Platinum 8270
- **Max MHz:** 4000
- **Nominal:** 2700
- **Enabled:** 52 cores, 2 chips
- **Orderable:** 1,2 chips
- **Cache L1:** 32 KB I+ D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 35.75 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 240 GB M.2 SATA SSD

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Power Management:** --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8270, 2.70GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>52</td>
<td>112</td>
<td>526</td>
<td>113</td>
<td>524</td>
<td>113</td>
<td>522</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>52</td>
<td>93.6</td>
<td>178</td>
<td>94.0</td>
<td>177</td>
<td>94.8</td>
<td>176</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>52</td>
<td>49.7</td>
<td>105</td>
<td>49.9</td>
<td>105</td>
<td>50.7</td>
<td>103</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>52</td>
<td>101</td>
<td>130</td>
<td>101</td>
<td>131</td>
<td>101</td>
<td>131</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>52</td>
<td>74.0</td>
<td>120</td>
<td>74.0</td>
<td>120</td>
<td>74.0</td>
<td>120</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>52</td>
<td>187</td>
<td>63.6</td>
<td>186</td>
<td>63.8</td>
<td>186</td>
<td>63.8</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>52</td>
<td>88.9</td>
<td>162</td>
<td>90.2</td>
<td>160</td>
<td>89.5</td>
<td>161</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>52</td>
<td>56.4</td>
<td>310</td>
<td>56.4</td>
<td>310</td>
<td>56.4</td>
<td>310</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>52</td>
<td>109</td>
<td>83.7</td>
<td>109</td>
<td>83.5</td>
<td>110</td>
<td>83.1</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>52</td>
<td>101</td>
<td>156</td>
<td>101</td>
<td>156</td>
<td>101</td>
<td>156</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8270, 2.70GHz)

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bdc091c0f
running on linux-pmqx Wed Aug 28 20:34:01 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8270 CPU @ 2.70GHz
2 "physical id"s (chips)
52 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 26
siblings : 26
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 52
On-line CPU(s) list: 0-51
Thread(s) per core: 1
Core(s) per socket: 26
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8270 CPU @ 2.70GHz
Stepping: 6
CPU MHz: 2700.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 5400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8270, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>151</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

| CPU2017 License: | 9019 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |
| Test Date: | Jul-2019 |
| Hardware Availability: | Apr-2019 |
| Software Availability: | May-2019 |

Platform Notes (Continued)

```plaintext
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-25
NUMA node1 CPU(s): 26-51
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtrunc pdcm ptil dca sse4_1 sse4_2 x2apic movbe popcnt
```

```
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdq停下来 intel_pni mba tpr_shadow vmni flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbms_local cqm_mbms_access
lpbb ibrs itlbpi stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd
```

```
From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
node 0 size: 385615 MB
node 0 free: 381147 MB
node 1 cpus: 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51
node 1 size: 387014 MB
node 1 free: 386333 MB
node distances:
node 0 1
0: 10 21
1: 21 10
```

```
From /proc/meminfo
MemTotal: 791173360 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

```
From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8270, 2.70GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Jul-2019</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

```
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
   Linux linux-pmqx 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
   x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Aug 28 15:55
SPEC is set to: /home/cpu2017
```

```
Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sdb4      btrfs  169G   18G  151G  11% /home
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
   24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

**Compiler Version Notes**

```
C     | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

```
C++, C, Fortran | 607.cactuBSSN_s(base)
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8270, 2.70GHz)

SPECSpeed®2017_fp_base = 151
SPECSpeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jul-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

------------------------------------------------------------------------------
| Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base) |
------------------------------------------------------------------------------
| Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) |
| 64, Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
------------------------------------------------------------------------------

------------------------------------------------------------------------------
| Fortran, C      | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base) |
------------------------------------------------------------------------------
| Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) |
| 64, Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
Version 19.0.4.227 Build 20190416 |
Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
------------------------------------------------------------------------------

Base CompilerInvocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl

(Continued on next page)
### SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**  
Cisco UCS B200 M5 (Intel Xeon Platinum 8270, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>151</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jul-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Base Portability Flags (Continued)

- 638.imagick_s: -DSPEC_LP64  
- 644.nab_s: -DSPEC_LP64  
- 649.fotonik3d_s: -DSPEC_LP64  
- 654.roms_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=4`  
- `-qopenmp`  
- `-DSPEC_OPENMP`

**Fortran benchmarks:**
- `-DSPEC_OPENMP`  
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=4`  
- `-qopenmp`  
- `-nstandard-realloc-lhs`

**Benchmarks using both Fortran and C:**
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=4`  
- `-qopenmp`  
- `-DSPEC_OPENMP`  
- `-nstandard-realloc-lhs`

**Benchmarks using Fortran, C, and C++:**
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=4`  
- `-qopenmp`  
- `-DSPEC_OPENMP`  
- `-nstandard-realloc-lhs`

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-08-28 23:34:00-0400.  
Originally published on 2019-09-19.

Page 7  
Standard Performance Evaluation Corporation (info@spec.org)  
https://www.spec.org/