Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6242, 2.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

spec

SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECspeed®2017_int_base = 10.1
SPECspeed®2017_int_peak = Not Run

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600.perlbench_s 32 6.81 10.1
602.gcc_s 32 9.65 12.5
605.mcf_s 32 7.28 14.4
620.omnetpp_s 32 5.45 14.4
623.xalancbmk_s 32 4.78 16.7
625.x264_s 32 23.0
631.deepsjeng_s 32 1.00 2.00
641.leela_s 32 1.00 2.00
648.exchange2_s 32 3.00 5.00
657.xz_s 32 5.00 7.00

--- SPECspeed®2017_int_base (10.1)

Hardware

CPU Name: Intel Xeon Gold 6242
Max MHz: 3900
Nominal: 2800
Enabled: 32 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 22 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 600 GB 10K RPM SAS
Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4b released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: --
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<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
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<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
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</tr>
</tbody>
</table>

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>32</td>
<td>259</td>
<td>6.85</td>
<td>261</td>
<td>6.81</td>
<td>261</td>
<td>6.81</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>32</td>
<td>413</td>
<td>9.65</td>
<td>413</td>
<td>9.64</td>
<td>412</td>
<td>9.65</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>32</td>
<td>376</td>
<td>12.5</td>
<td>377</td>
<td>12.5</td>
<td>376</td>
<td>12.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>32</td>
<td>224</td>
<td>7.28</td>
<td>225</td>
<td>7.26</td>
<td>222</td>
<td>7.34</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>32</td>
<td>114</td>
<td>12.4</td>
<td>114</td>
<td>12.4</td>
<td>115</td>
<td>12.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>625.x264_s</td>
<td>32</td>
<td>122</td>
<td>14.4</td>
<td>122</td>
<td>14.4</td>
<td>122</td>
<td>14.4</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>32</td>
<td>263</td>
<td>5.44</td>
<td>263</td>
<td>5.45</td>
<td>263</td>
<td>5.46</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>641.leela_s</td>
<td>32</td>
<td>357</td>
<td>4.78</td>
<td>356</td>
<td>4.79</td>
<td>357</td>
<td>4.78</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>32</td>
<td>176</td>
<td>16.7</td>
<td>178</td>
<td>16.5</td>
<td>176</td>
<td>16.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>657.xz_s</td>
<td>32</td>
<td>273</td>
<td>22.7</td>
<td>273</td>
<td>22.7</td>
<td>273</td>
<td>22.6</td>
<td></td>
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</tbody>
</table>

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

## SPEC CPU®2017 Integer Speed Result

### Cisco Systems

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<tbody>
<tr>
<td>SPECspeed®2017_int_peak</td>
<td>Not Run</td>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes

BIOS Settings:
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- IMC Interleaving set to Auto
- Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
runtime on linux-k1c6 Thu Aug 29 01:16:53 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
- 2 "physical id"s (chips)
- 32 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
- cpu cores: 16
- siblings: 16
- physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
- physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 32
- On-line CPU(s) list: 0-31
- Thread(s) per core: 1
- Core(s) per socket: 16
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
- Stepping: 6
- CPU MHz: 2800.000
- CPU max MHz: 3900.0000
- CPU min MHz: 1200.0000
- BogoMIPS: 5600.00
- Virtualization: VT-x
- L1d cache: 32K

(Continued on next page)
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Platform Notes (Continued)

<table>
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<tr>
<th>Cache Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1i cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache:</td>
<td>1024K</td>
</tr>
<tr>
<td>L3 cache:</td>
<td>22528K</td>
</tr>
</tbody>
</table>

NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31

Flags:
- fpu vmx de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
- pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
- lm constant-tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
- aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
- sdbg fma cx16 xtpre pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
- tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
- epb cat_13 cdp_13 invpcid_single intel_puin mba tpr_shadow vmni priority ept
- vpid fsgsbase tsc_adjust bmis hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
- avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
- xsaveopt xsave xgetbv1 xsaves cqm_llc cqm_occupa llc cqm_mbms_total cqm_mbms_local
- ibpb ibrs ibsr ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
- ospke avx512_vni arch_capabilities ssbd

/proc/cpuinfo cache data
- cache size : 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
- available: 2 nodes (0-1)
  - node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  - node 0 size: 385429 MB
  - node 0 free: 384099 MB
  - node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
  - node 1 size: 387045 MB
  - node 1 free: 383382 MB
  - node distances:
    - node 0 1: 10 21
    - node 1 0: 21 10

From /proc/meminfo
- MemTotal: 791014156 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
- os-release:
  - NAME="SLES"
  - VERSION="15"
  - VERSION_ID="15"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15"
  - ID="sles"

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Platform Notes (Continued)

ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-k1c6 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 28 22:56
SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdc2 btrfs 557G 18G 539G 4% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)                        |
|         | 625.x264_s(base) 657.xz_s(base)                                               |
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
| C++     | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)               |
|         | 641.leela_s(base)                                                            |
==============================================================================

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
| Fortran | 648.exchange2_s(base)                                                        |
==============================================================================
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Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64  -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64

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### Base Optimization Flags (Continued)

C++ benchmarks (continued):
- -lqkmalloc

Fortran benchmarks:
- -xCORE-AVX512
- -ipo
- -O3
- -no-prec-div
- -qopt-mem-layout-trans=4
- -nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links: