Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4208, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>82.4</th>
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<tr>
<td>SPECrate®2017_int_peak</td>
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</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
** Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Hardware
- **CPU Name:** Intel Xeon Silver 4208
- **Max MHz:** 3200
- **Nominal:** 2100
- **Enabled:** 16 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 11 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
- **Storage:** 1 x 600 GB 10K RPM SAS
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --
**Cisco Systems**  
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<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
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<th>Ratio</th>
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<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>32</td>
<td>815</td>
<td>62.5</td>
<td>814</td>
<td>62.6</td>
<td>817</td>
<td>62.4</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>32</td>
<td>660</td>
<td>68.7</td>
<td>667</td>
<td>68.0</td>
<td>660</td>
<td>68.7</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>32</td>
<td>462</td>
<td>112</td>
<td>464</td>
<td>112</td>
<td>462</td>
<td>112</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>32</td>
<td>743</td>
<td>56.5</td>
<td>741</td>
<td>56.6</td>
<td>742</td>
<td>56.6</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>32</td>
<td>359</td>
<td>94.0</td>
<td>360</td>
<td>94.0</td>
<td>359</td>
<td>94.1</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>32</td>
<td>381</td>
<td>147</td>
<td>379</td>
<td>148</td>
<td>372</td>
<td>150</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>32</td>
<td>539</td>
<td>68.1</td>
<td>539</td>
<td>68.1</td>
<td>539</td>
<td>68.1</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>32</td>
<td>855</td>
<td>62.0</td>
<td>853</td>
<td>62.2</td>
<td>854</td>
<td>62.1</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>32</td>
<td>511</td>
<td>164</td>
<td>511</td>
<td>164</td>
<td>508</td>
<td>165</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>32</td>
<td>629</td>
<td>54.9</td>
<td>630</td>
<td>54.9</td>
<td>630</td>
<td>54.9</td>
</tr>
</tbody>
</table>

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Test Date: Aug-2019  
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**Results Table**

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**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**General Notes**

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3>/proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

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General Notes (Continued)

is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bce091c0f
running on linux-k1c6 Fri Aug 30 20:54:10 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000

(Continued on next page)
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SPECrater®2017_int_base = 82.4
SPECrater®2017_int_peak = Not Run

Platform Notes (Continued)

CPU max MHz: 3200.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdkg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_13 invpcid_single intel_pinin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbms_total cqm_mbms_local
lbpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

From /proc/cpuinfo cache data
- cache size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
- available: 2 nodes (0-1)
- node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
- node 0 size: 386402 MB
- node 0 free: 385820 MB
- node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
- node 1 size: 387016 MB
- node 1 free: 386527 MB
- node distances:
  - node 0 1
  - 0: 10 21
  - 1: 21 10

From /proc/meminfo
- MemTotal: 791980808 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
- os-release:

(Continued on next page)
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Platform Notes (Continued)

NAME="SLES"
VERSION=""15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-k1c6 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Aug 30 20:44
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdc2 btrfs 557G 15G 542G 3% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory: 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

Compiler Version Notes

C  | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
   | 525.x264_r(base) 557.xz_r(base)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++  | 520.omnetpp_r(base) 523.xalancbk_r(base) 531.deepsjeng_r(base)
     | 541.leela_r(base)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416

(Continued on next page)
# SPEC CPU®2017 Integer Rate Result

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## Compiler Version Notes (Continued)

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
Fortran | 548.exchange2_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

## Base Compiler Invocation

**C benchmarks:**
icc -m64 -std=c11

**C++ benchmarks:**
icpc -m64

**Fortran benchmarks:**
ifort -m64

## Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

## Base Optimization Flags

**C benchmarks:**
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64

(Continued on next page)
## Base Optimization Flags (Continued)

C benchmarks (continued):
- `-lqkmalloc`

C++ benchmarks:
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

Fortran benchmarks:
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-nostandard-realloc-lhs`
- `-align array32byte`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-08-30 23:54:09-0400.
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