## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3204, 1.90GHz)

| SPECspeed®2017_fp_base = 43.8 | SPECspeed®2017_fp_peak = Not Run |

| CPU2017 License: 9019 | Test Date: Aug-2019 |
| Test Sponsor: Cisco Systems | Hardware Availability: Apr-2019 |
| Tested by: Cisco Systems | Software Availability: May-2019 |

### Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>12</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>12</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>12</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>12</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>12</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>12</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>12</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>12</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>12</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>12</td>
</tr>
</tbody>
</table>

### Hardware

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name:</td>
<td>Intel Xeon Bronze 3204</td>
</tr>
<tr>
<td>Max MHz:</td>
<td>1900</td>
</tr>
<tr>
<td>Nominal:</td>
<td>1900</td>
</tr>
<tr>
<td>Enabled:</td>
<td>12 cores, 2 chips</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1,2 chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I+ 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3:</td>
<td>8.25 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Memory:</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2133)</td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 240 GB M.2 SATA SSD</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
</tbody>
</table>

### Software

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS:</td>
<td>SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
</tr>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux</td>
</tr>
<tr>
<td>Parallel:</td>
<td>Yes</td>
</tr>
<tr>
<td>Firmware:</td>
<td>Version 4.0.4b released Apr-2019</td>
</tr>
<tr>
<td>File System:</td>
<td>btrfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Power Management:</td>
<td>--</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3204, 1.90GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_fp_base = 43.8
SPECspeed®2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>12</td>
<td>258</td>
<td>229</td>
<td>258</td>
<td>229</td>
<td>259</td>
<td>228</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>12</td>
<td>347</td>
<td>48.0</td>
<td>347</td>
<td>48.0</td>
<td>347</td>
<td>48.0</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>12</td>
<td>148</td>
<td>35.4</td>
<td>148</td>
<td>35.4</td>
<td>148</td>
<td>35.3</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>12</td>
<td>308</td>
<td>42.9</td>
<td>307</td>
<td>43.1</td>
<td>309</td>
<td>42.9</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>12</td>
<td>444</td>
<td>20.0</td>
<td>444</td>
<td>20.0</td>
<td>445</td>
<td>19.9</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>12</td>
<td>346</td>
<td>34.3</td>
<td>348</td>
<td>34.1</td>
<td>346</td>
<td>34.3</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>12</td>
<td>561</td>
<td>25.7</td>
<td>561</td>
<td>25.7</td>
<td>560</td>
<td>25.8</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>12</td>
<td>366</td>
<td>47.8</td>
<td>366</td>
<td>47.8</td>
<td>366</td>
<td>47.8</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>12</td>
<td>208</td>
<td>43.9</td>
<td>208</td>
<td>43.7</td>
<td>209</td>
<td>43.7</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>12</td>
<td>372</td>
<td>42.3</td>
<td>372</td>
<td>42.3</td>
<td>373</td>
<td>42.2</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
    numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3204, 1.90GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_fp_base = 43.8
SPECspeed®2017_fp_peak = Not Run

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-5vrl Sun Sep 1 00:05:38 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Bronze 3204 CPU @ 1.90GHz
  2 "physical id"s (chips)
  12 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores: 6
  siblings: 6
  physical 0: cores 0 1 2 3 4 5
  physical 1: cores 0 1 2 3 4 5

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 12
On-line CPU(s) list: 0-11
Thread(s) per core: 1
Core(s) per socket: 6
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Bronze 3204 CPU @ 1.90GHz
Stepping: 6
CPU MHz: 1900.000
CPU max MHz: 1900.0000
CPU min MHz: 800.0000
BogoMIPS: 3800.00
Virtualization: VT-x
L1d cache: 32K

(Continued on next page)
## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Bronze 3204, 1.90GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>43.8</th>
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</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
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9019

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Cisco Systems

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---

### Platform Notes (Continued)

- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 8448K
- NUMA node0 CPU(s): 0-5
- NUMA node1 CPU(s): 6-11
- Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pmm mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local ibpb ibrs stibp dtherm arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
- cache size : 8448 KB

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

- available: 2 nodes (0-1)
- node 0 cpus: 0 1 2 3 4 5
- node 0 size: 385590 MB
- node 0 free: 381954 MB
- node 1 cpus: 6 7 8 9 10 11
- node 1 size: 387047 MB
- node 1 free: 380886 MB
- node distances:
  - node 0: 10 21
  - node 1: 21 10

From /proc/meminfo

- MemTotal: 791181076 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

- os-release:
  - NAME="SLES"
  - VERSION="15"
  - VERSION_ID="15"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15"
  - ID="sles"

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Platform Notes (Continued)

ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-5vrl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 31 11:44
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb1 btrfs 224G 22G 201G 10% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2133

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
 64, Version 19.0.4.227 Build 20190416
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Compiler Version Notes (Continued)

---------------------------------------------------------------------
Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
---------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
---------------------------------------------------------------------
Fortran, C      | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
---------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
---------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
   -assume byterecl
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Base Portability Flags (Continued)

638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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