Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

<table>
<thead>
<tr>
<th>Copies</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td></td>
</tr>
<tr>
<td>508.namd_r</td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td></td>
</tr>
<tr>
<td>511.povray_r</td>
<td></td>
</tr>
<tr>
<td>519.lbm_r</td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td></td>
</tr>
<tr>
<td>526.blender_r</td>
<td></td>
</tr>
<tr>
<td>527.cam4_r</td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td></td>
</tr>
</tbody>
</table>

### Hardware

Max MHz: 3000
Nominal: 2200
Enabled: 32 cores, 2 chips, 2 threads/core
Orderable: 1,2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 22 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 240 GB M.2 SATA SSD
Other: None

### Software

OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4b released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: --
Non-compliant

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
</tbody>
</table>

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**General Notes**

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)
SPECrate®2017_fp_peak =
SPECrate®2017_fp_base =

SPECSPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

General Notes (Continued)
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation:
Filesystem page cache synced and cleared with:

sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU Performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz
2 "physical id"s (chips)
64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

(Continued on next page)
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

cpu cores : 16  
siblings : 32  
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15  
physical 1: cores 0 1 2 3 4 5 6 7 8 10 11 12 13 14 15  

From lscpu:
Architecture: x86_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  

CPU(s): 64  
On-line CPU(s) list: 0-63  
Thread(s) per core: 2  
Core(s) per socket: 16  
Socket(s): 2  
NUMA node(s): 4  
Vendor ID: GenuineIntel  
CPU family: 6  
Model: 85  
Model name: Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz  
Stepping: 6  
CPU MHz: 2200.000  
CPU max MHz: 3000.0000  
CPU min MHz: 1000.0000  
Cache: 4400.00  
Virtualization: VT-x  
L1d cache: 32K  
L1i cache: 32K  
L2 cache: 1024K  
L3 cache: 22528K  
NUMA node0 CPU(s): 0-3,8-11,32-35,40-43  
NUMA node1 CPU(s): 4-7,12-15,36-39,44-47  
NUMA node2 CPU(s): 16-19,24-27,48-51,56-59  
NUMA node3 CPU(s): 20-23,28-31,52-55,60-63  
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

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Platform Notes (Continued)

sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdtscp lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_pmln mba tpr_shadow vmi flexpriority ept
tpid fsgsbase tsc_adjust bmi1 intel_p8洪 btri aemms mtrre cmov cx8

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 8 9 10 11 32 33 34 35 40 41 42 43
node 0 size: 191903 MB
node 0 free: 190665 MB
node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
node 1 size: 193522 MB
node 1 free: 193031 MB
node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
node 2 size: 193522 MB
node 2 free: 192997 MB
node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
node 3 size: 193519 MB
node 3 free: 193049 MB
node distances:
node

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

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Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-db10 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 26 10:15

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 52G 170G 24% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrate®2017.fp_base =
SPECrate®2017.fp_peak =

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jul-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

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Platform Notes (Continued)
(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) C</td>
<td>Intel(R) 64 Compiler for applications running on Intel(R) 64,</td>
</tr>
<tr>
<td></td>
<td>Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td></td>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>-----------------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>C++</td>
<td>508.namd_r(base) 510.parest_r(base)</td>
</tr>
<tr>
<td>-----------------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>Intel(R) C++</td>
<td>Intel(R) 64 Compiler for applications running on Intel(R) 64,</td>
</tr>
<tr>
<td></td>
<td>Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td>-----------------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>C++, C</td>
<td>511.povray_r(base) 526.blender_r(base)</td>
</tr>
<tr>
<td>-----------------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>Intel(R) C++</td>
<td>Intel(R) 64 Compiler for applications running on Intel(R) 64,</td>
</tr>
<tr>
<td></td>
<td>Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td>-----------------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>C++, C, Fortran</td>
<td>507.cactuBSSN_r(base)</td>
</tr>
<tr>
<td>-----------------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>Intel(R) C++</td>
<td>Intel(R) 64 Compiler for applications running on Intel(R) 64,</td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td></td>
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</tr>
</tbody>
</table>

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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

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Compiler Version Notes (Continued)
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) C Intel (R) 64 Compiler for applications running on Intel (R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation
C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base =</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak =</td>
</tr>
</tbody>
</table>

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**Base Compiler Invocation (Continued)**

Fortran benchmarks:
```bash
ifort -m64
```

Benchmarks using both Fortran and C:
```bash
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:
```bash
icpc -m64 icc -m64 -std=c
```

Benchmarks using Fortran, C, and C++:
```bash
icpc -m64 icc -m64 -std=c11 ifort -m64
```

**Base Portability Flags**

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.navd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.ibm_r: -DSPEC_LP64
- 520.blender_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 521.cam4_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 523.mGRID_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 525.raytrace_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.foton3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
```bash
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
```

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

### Cisco Systems

**Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)**

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

- **Test Date:** Jul-2019  
- **Hardware Availability:** Apr-2019  
- **Software Availability:** May-2019

### Base Optimization Flags (Continued)

C benchmarks (continued):
- `-ffinite-math-only -qopt-mem-layout-tran=1`

C++ benchmarks:
- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-tran=4`

Fortran benchmarks:
- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-tran=4 -auto`
- `-nostandard-realloc-lhs -align array32byte`

Benchmarks using both Fortran and C:
- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-tran=4 -auto`
- `-nostandard-realloc-lhs -align array32byte`

Benchmarks using both C++ and C:
- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-tran=4`

Benchmarks using Fortran, C, and C++:
- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-tran=4 -auto`
- `-nostandard-realloc-lhs -align array32byte`

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


---

**SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.**
<table>
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<tr>
<th>SPEC CPU®2017 Floating Point Rate Result</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
</tbody>
</table>

Cisco Systems  
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)  
SPECrater®2017_fp_peak =  
SPECrater®2017_fp_base =

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Jul-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
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