Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6226, 2.70GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPECrate®2017_fp_base = 167
SPECrate®2017_fp_peak = 170

Hardware
CPU Name: Intel Xeon Gold 6226
Max MHz: 3700
Nominal: 2700
Enabled: 24 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 19.25 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4c released Apr-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: --
SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6226, 2.70GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 167
SPECrate®2017_fp_peak = 170

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>48</td>
<td>1045</td>
<td>461</td>
<td>1046</td>
<td>460</td>
<td>1046</td>
<td>460</td>
<td>48</td>
<td>1045</td>
<td>460</td>
<td>1045</td>
<td>460</td>
<td>1045</td>
<td>460</td>
<td></td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>48</td>
<td>512</td>
<td>119</td>
<td>511</td>
<td>119</td>
<td>511</td>
<td>119</td>
<td>48</td>
<td>511</td>
<td>119</td>
<td>511</td>
<td>119</td>
<td>511</td>
<td>119</td>
<td></td>
<td></td>
</tr>
<tr>
<td>508.namd_r</td>
<td>48</td>
<td>385</td>
<td>118</td>
<td>384</td>
<td>119</td>
<td>384</td>
<td>119</td>
<td>48</td>
<td>382</td>
<td>119</td>
<td>381</td>
<td>120</td>
<td>381</td>
<td>120</td>
<td></td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td>48</td>
<td>1223</td>
<td>103</td>
<td>1224</td>
<td>103</td>
<td>1227</td>
<td>102</td>
<td>48</td>
<td>1225</td>
<td>103</td>
<td>1223</td>
<td>103</td>
<td>1224</td>
<td>103</td>
<td></td>
<td></td>
</tr>
<tr>
<td>511.povray_r</td>
<td>48</td>
<td>640</td>
<td>175</td>
<td>650</td>
<td>173</td>
<td>649</td>
<td>173</td>
<td>48</td>
<td>546</td>
<td>205</td>
<td>548</td>
<td>205</td>
<td>548</td>
<td>205</td>
<td></td>
<td></td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>48</td>
<td>484</td>
<td>104</td>
<td>484</td>
<td>104</td>
<td>485</td>
<td>104</td>
<td>48</td>
<td>484</td>
<td>105</td>
<td>484</td>
<td>105</td>
<td>484</td>
<td>105</td>
<td></td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>48</td>
<td>586</td>
<td>184</td>
<td>582</td>
<td>185</td>
<td>572</td>
<td>188</td>
<td>48</td>
<td>563</td>
<td>191</td>
<td>569</td>
<td>189</td>
<td>538</td>
<td>200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>526.blender_r</td>
<td>48</td>
<td>449</td>
<td>163</td>
<td>449</td>
<td>163</td>
<td>448</td>
<td>163</td>
<td>48</td>
<td>448</td>
<td>163</td>
<td>449</td>
<td>163</td>
<td>449</td>
<td>163</td>
<td></td>
<td></td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>48</td>
<td>478</td>
<td>176</td>
<td>479</td>
<td>175</td>
<td>488</td>
<td>172</td>
<td>48</td>
<td>471</td>
<td>178</td>
<td>475</td>
<td>177</td>
<td>471</td>
<td>178</td>
<td></td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>48</td>
<td>326</td>
<td>367</td>
<td>326</td>
<td>366</td>
<td>325</td>
<td>367</td>
<td>48</td>
<td>327</td>
<td>365</td>
<td>326</td>
<td>366</td>
<td>327</td>
<td>365</td>
<td></td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td>48</td>
<td>306</td>
<td>264</td>
<td>309</td>
<td>261</td>
<td>306</td>
<td>264</td>
<td>48</td>
<td>307</td>
<td>263</td>
<td>310</td>
<td>261</td>
<td>307</td>
<td>263</td>
<td></td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>48</td>
<td>1295</td>
<td>144</td>
<td>1292</td>
<td>145</td>
<td>1296</td>
<td>144</td>
<td>48</td>
<td>1293</td>
<td>145</td>
<td>1294</td>
<td>145</td>
<td>1295</td>
<td>144</td>
<td></td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>48</td>
<td>860</td>
<td>88.7</td>
<td>863</td>
<td>88.4</td>
<td>858</td>
<td>88.9</td>
<td>48</td>
<td>858</td>
<td>88.9</td>
<td>861</td>
<td>88.6</td>
<td>861</td>
<td>88.6</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6226, 2.70GHz)

SPEC CPU 2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrater®2017_fp_base = 167
SPECrater®2017_fp_peak = 170

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-4z0x Sat Aug 31 12:32:47 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6226 CPU @ 2.70GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
  siblings : 24
  physical 0: cores 0 2 3 4 6 8 9 10 11 12 13 14
  physical 1: cores 1 2 3 5 6 8 9 10 11 12 13 14

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6226 CPU @ 2.70GHz
Stepping: 7

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6226, 2.70GHz)

SPECrate®2017_fp_base = 167
SPECrate®2017_fp_peak = 170

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

CPU MHz: 2700.000
CPU max MHz: 3700.0000
CPU min MHz: 1200.0000
BogoMIPS: 5400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 19712K
NUMA node0 CPU(s): 0-2,5-7,24-26,29-31
NUMA node1 CPU(s): 3,4,8-11,27,28,32-35
NUMA node2 CPU(s): 12-14,17-19,36-38,41-43
NUMA node3 CPU(s): 15,16,20-23,39,40,44-47
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology

/proc/cpuinfo cache data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6226, 2.70GHz)

SPECrate®2017_fp_base = 167
SPECrate®2017_fp_peak = 170

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: May-2019

Platform Notes (Continued)

1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791202036 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-4z0x 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 31 04:41

SPEC is set to: /home/cpu2017

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.4c.0.0411190411 04/11/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6226, 2.70GHz)  
SPECrater®2017_fp_base = 167
SPECrater®2017_fp_peak = 170

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Test Date: Aug-2019  
Tested by: Cisco Systems  
Hardware Availability: Apr-2019  
Software Availability: May-2019

Compiler Version Notes

==============================================================================
| C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)  
|                 | 544.nab_r(base, peak) |
-----------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----------------------------------------------------------------------------

==============================================================================
| C++             | 508.namd_r(base, peak) 510.parest_r(base, peak) |
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----------------------------------------------------------------------------

==============================================================================
| C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak) |
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----------------------------------------------------------------------------

==============================================================================
| C++, C, Fortran | 507.cactuBSSN_r(base, peak) |
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----------------------------------------------------------------------------

==============================================================================
| Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)  
|                 | 554.roms_r(base, peak) |
-----------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6226, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 167</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 170</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
-----------------|---------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6226, 2.70GHz)  

| SPECrate®2017_fp_base = 167 |
| SPECrate®2017_fp_peak = 170 |

| CPU2017 License: 9019 | Test Date: Aug-2019 |
| Test Sponsor: Cisco Systems | Hardware Availability: Apr-2019 |
| Tested by: Cisco Systems | Software Availability: May-2019 |

### Base Portability Flags (Continued)

- `521.wrf_r`: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
- `526.blender_r`: `-DSPEC_LP64 -DSPEC_LINUX -funsigned-char`
- `527.cam4_r`: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
- `538.imagick_r`: `-DSPEC_LP64`
- `544.nab_r`: `-DSPEC_LP64`
- `549.fotonik3d_r`: `-DSPEC_LP64`
- `554.roms_r`: `-DSPEC_LP64`

### Base Optimization Flags

#### C benchmarks:

- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=4`

#### C++ benchmarks:

- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=4`

#### Fortran benchmarks:

- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=4 -auto`
- `-nostandard-realloc-lhs -align array32byte`

#### Benchmarks using both Fortran and C:

- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=4 -auto`
- `-nostandard-realloc-lhs -align array32byte`

#### Benchmarks using both C and C++:

- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=4`

#### Benchmarks using Fortran, C, and C++:

- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=4 -auto`
- `-nostandard-realloc-lhs -align array32byte`

### Peak Compiler Invocation

#### C benchmarks:

- `icc -m64 -std=c11`

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6226, 2.70GHz)

SPECrate®2017_fp_base = 167
SPECrate®2017_fp_peak = 170

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

538.imagick_r -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:
508.namd_r -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6226, 2.70GHz)

| SPECrate\textsuperscript{®}2017\_fp\_base | 167 |
| SPECrate\textsuperscript{®}2017\_fp\_peak | 170 |

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

---

### Peak Optimization Flags (Continued)

**Fortran benchmarks:**

- 503.bwaves\_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -auto  
-nostandard-realloc-lhs -align array32byte  
-549.fotonik3d\_r: Same as 503.bwaves\_r  
-554.roms\_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs  
-align array32byte

**Benchmarks using both Fortran and C:**

- -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs  
-align array32byte

**Benchmarks using both C and C++:**

- 511.povray\_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4  
-526.blender\_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4

**Benchmarks using Fortran, C, and C++:**

- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -auto  
-nostandard-realloc-lhs -align array32byte

---

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:

## Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6226, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>167</td>
<td>170</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Sponsor</th>
<th>Tested by</th>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
</table>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-08-31 03:02:46-0400.
Originally published on 2019-09-19.