## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4214, 2.20GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 136</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak = 141</td>
</tr>
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</table>

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Firmware:** Version 4.0.4d released May-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --

### Hardware

- **CPU Name:** Intel Xeon Silver 4214
- **Max MHz:** 3200
- **Nominal:** 2200
- **Enabled:** 24 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 16.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Test Details

- **CPU2017 License:** 9019
- **Test Sponsor:** Cisco Systems
- **Tested by:** Cisco Systems
- **Test Date:** Aug-2019
- **Hardware Availability:** Apr-2019
- **Software Availability:** May-2019

### Benchmark Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
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<tr>
<td>perlbench_r</td>
<td>48</td>
<td>118</td>
<td>141</td>
</tr>
<tr>
<td>gcc_r</td>
<td>48</td>
<td>113</td>
<td>141</td>
</tr>
<tr>
<td>mcf_r</td>
<td>48</td>
<td>93.4</td>
<td>141</td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>48</td>
<td>93.5</td>
<td>141</td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>48</td>
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</tr>
<tr>
<td>x264_r</td>
<td>48</td>
<td>170</td>
<td>141</td>
</tr>
<tr>
<td>deepsjeng_r</td>
<td>48</td>
<td>111</td>
<td>141</td>
</tr>
<tr>
<td>leela_r</td>
<td>48</td>
<td>100</td>
<td>141</td>
</tr>
<tr>
<td>exchange2_r</td>
<td>48</td>
<td>101</td>
<td>141</td>
</tr>
<tr>
<td>xz_r</td>
<td>48</td>
<td>90.3</td>
<td>141</td>
</tr>
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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4214, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

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<tr>
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<th>Copies</th>
<th>Seconds</th>
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<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>48</td>
<td>748</td>
<td>102</td>
<td>746</td>
<td>102</td>
<td>753</td>
<td>101</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>48</td>
<td>601</td>
<td>113</td>
<td>599</td>
<td>113</td>
<td>591</td>
<td>115</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>48</td>
<td>422</td>
<td>184</td>
<td>425</td>
<td>183</td>
<td>422</td>
<td>184</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>48</td>
<td>673</td>
<td>93.6</td>
<td>674</td>
<td>93.4</td>
<td>675</td>
<td>93.4</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>48</td>
<td>318</td>
<td>159</td>
<td>317</td>
<td>160</td>
<td>318</td>
<td>159</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>48</td>
<td>321</td>
<td>262</td>
<td>321</td>
<td>262</td>
<td>321</td>
<td>261</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>48</td>
<td>497</td>
<td>111</td>
<td>497</td>
<td>111</td>
<td>498</td>
<td>111</td>
</tr>
<tr>
<td>541.leea_r</td>
<td>48</td>
<td>791</td>
<td>100</td>
<td>791</td>
<td>100</td>
<td>784</td>
<td>101</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>48</td>
<td>474</td>
<td>266</td>
<td>474</td>
<td>265</td>
<td>474</td>
<td>266</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>48</td>
<td>574</td>
<td>90.2</td>
<td>574</td>
<td>90.3</td>
<td>574</td>
<td>90.3</td>
</tr>
</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
General Notes (Continued)

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-3c6s Tue Aug 27 14:20:39 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 24
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
Stepping: 6
CPU MHz: 2200.000
SPEC CPU®2017 Integer Rate Result
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Cisco Systems
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SPECrate®2017_int_base = 136
SPECrate®2017_int_peak = 141

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

CPU max MHz: 3200.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 16896K
NUMA node0 CPU(s): 0-2,6-8,24-26,30-32
NUMA node1 CPU(s): 3-5,9-11,27-29,33-35
NUMA node2 CPU(s): 12-14,18-20,36-38,42-44
NUMA node3 CPU(s): 15-17,21-23,39-41,45-47
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pmm tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ermv invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

 available: 4 nodes (0-3)
node 0 cpus: 0 1 2 6 7 8 24 25 26 30 31 32
node 0 size: 192103 MB
node 0 free: 191775 MB
node 1 cpus: 3 4 5 9 10 11 27 28 29 33 34 35
node 1 size: 193528 MB
node 1 free: 193210 MB
node 2 cpus: 12 13 14 18 19 20 36 37 38 42 43 44
node 2 size: 193528 MB
node 2 free: 193314 MB
node 3 cpus: 15 16 17 21 22 23 39 40 41 45 46 47
node 3 size: 193497 MB
node 3 free: 193232 MB
node distances:
node 0 1 2 3
  0: 10 11 21 21
  1: 11 10 21 21

(Continued on next page)
Cisco Systems
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```
2:  21  21  10  11
3:  21  21  11  10

From /proc/meminfo
MemTotal:       791201996 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
   os-release:
      NAME="SLES"
      VERSION="15"
      VERSION_ID="15"
      PRETTY_NAME="SUSE Linux Enterprise Server 15"
      ID="sles"
      ID_LIKE="suse"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
   Linux linux-3c6s 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown):          Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 27 14:09

SPEC is set to: /home/cpu2017
   Filesystem     Type  Size  Used Avail Use% Mounted on
   /dev/sda1      xfs   224G   20G  204G   9% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
   Memory:
      24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)
```
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- **Tested by:** Cisco Systems  
- **Test Date:** Aug-2019  
- **Hardware Availability:** Apr-2019  
- **Software Availability:** May-2019

### Compiler Version Notes

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<th>C</th>
<th>502.gcc_r(peak)</th>
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| Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416  
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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4214, 2.20GHz)

SPEC CPU®2017 Integer Rate Result

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Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
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------------------------------------------------------------------------------
C++ | 523.xalancbmk_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
    | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

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Base Portability Flags (Continued)

502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11

-spec_r: icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

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Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

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Test Date: Aug-2019
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Peak Optimization Flags (Continued)

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/jemalloc-5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-08-27 04:50:38-0400.
Originally published on 2019-09-19.