Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

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<td>505.mcf_r</td>
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<td>523.xalancbmk_r</td>
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<tr>
<td>548.exchange2_r</td>
</tr>
<tr>
<td>557.xz_r</td>
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</table>

**Hardware**
- **CPU Name:** Intel Xeon Platinum 8253
- **Max MHz:** 3000
- **Nominal:** 2200
- **Enabled:** 32 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 22 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

**Software**
- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4d released May-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

### Results Table

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</tbody>
</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrare®2017_int_base =
SPECrare®2017_int_peak =

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

General Notes (Continued)

Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Version: 2018-05-19 9bcd8f2999c33d6f64985e4585ea9
Running on linux-3c6s Wed Aug 21 13:00:10 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16

(Continued on next page)
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture:        x86_64
CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
CPU(s):              64
On-line CPU(s) list: 0-63
Thread(s) per core:  2
Core(s) per socket:  16
Socket(s):           2
NUMA node(s):        4
Vendor ID:           GenuineIntel
CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz
Stepping:            6
CPU MHz:             2200.000
CPU max MHz:         3000.0000
CPU min MHz:         1000.0000
BogoMIPS:            4400.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            22528K
NUMA node0 CPU(s):   0-3,8-11,32-35,40-43
NUMA node1 CPU(s):   4-7,12-15,36-39,44-47
NUMA node2 CPU(s):   16-19,24-27,48-51,56-59
NUMA node3 CPU(s):   20-23,28-31,52-55,60-63
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
                     pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
                     lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
                     aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
                     sdbg fma cx16 xtopr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

| SPECrate®2017_int_base = |
| SPECrate®2017_int_peak = |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Non-Compliant

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

```
tsc_deadline_timer aes xsave avx f16c npred arhahf_lan abm 3dnwpmecp cuda Faults smpbase tsc_adjust bmi1 mtm2 bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed fux smm clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local ibpb ibrs ibsr dtherm ida arat pbes hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd
```

```
/proc/cpuinfo cache data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 8 9 10 11 32 33 34 35 40 41 42 43
node 0 size: 192102 MB
node 0 free: 191661 MB
node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
node 1 size: 193527 MB
node 1 free: 193197 MB
node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
node 2 size: 193527 MB
node 2 free: 193300 MB
node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
node 3 size: 193497 MB
node 3 free: 193268 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791198916 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

(Continued on next page)
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

From /etc/*release* /etc/*version*

```
From /etc/*release*/etc/*version*
 os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
 Linux linux-3c6s-4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5755 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW
```
```
Aug 21 12:58
```

```
SPEC is set to: /home/cpu2017
 Filesystem Type Size Used Avail Use% Mounted on
 /dev/sdal xfs 224G 20G 204G 9% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)
(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C   | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C   | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
    | 525.x264_r(base, peak) 557.xz_r(base, peak)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C   | 502.gcc_r(peak)
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C   | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
    | 525.x264_r(base, peak) 557.xz_r(base, peak)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

Non-Compliant
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.
SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPEC CPU®2017_int_base =
SPEC CPU®2017_int_peak =

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Compiler Version Notes (Continued)

==============================================================================
C++ | 523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)

| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C++ | 523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)

| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
Fortran | 548.exchange2_r(base, peak)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Compiler Version Notes (Continued)
-----------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation
-------------------------
C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags
---------------------
500.perlbench_r -DSPEC_LP64 -DSPEC_LINUX_X64
505.mcf_r -DSPEC_LP64
520.omnetpp_r -DSPEC_LP64
531.deepjeng_r -DSPEC_LP64 -DSPEC_LINUX
523.xalancbmk_r -DSPEC_LP64
548.exchange2_r -DSPEC_LP64
557.xz_r: -DSPEC_LP64
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

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**SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.**

### Base Optimization Flags

C benchmarks:
```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -m64 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

C++ benchmarks:
```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

Fortran benchmarks:
```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

### Peak Compiler Invocation

C benchmarks (except as noted below):
```
icc -m64 -std=c11
```

C++ benchmarks (except as noted below):
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalanbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-foo-strict-overflow
-I/usr/local/Intel Compiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

520.gcc_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-I/usr/local/jc5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-I/usr/local/Intel Compiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-I/usr/local/Intel Compiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Peak Optimization Flags (Continued)

557.xz_r: Same as 505.mcf_r

C++ benchmarks:
523.xalancbmk_r: -Wl,-z,muldefs,-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib -ljemalloc
531.deepsjeng_r: Same as 520.omnetpp_r
541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
Cisco Systems  
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