Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
  4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4d released May-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None

**Power Management:** --

**Non-Compliant**

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.
## SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**  
Cisco UCS C240 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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**SPECspeed®2017_fp_base =**

**SPECspeed®2017_fp_peak =**

**CPU2017 License:** 9019  
**Test Date:** Aug-2019  
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### Results Table

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```bash
sync; echo 3>/proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
**SPEC CPU®2017 Floating Point Speed Result**

***Cisco Systems***

Cisco UCS C240 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  

**General Notes (Continued)**

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

---

**Platform Notes**

- BIOS Settings:
  - Intel HyperThreading Technology set to Disabled
  - CPU performance set to Enterprise
  - Power Performance Tuning set to OS Controls
  - SNC set to Disabled
  - Patrol Scrub set to Disabled
- Sysinfo program: /home/cpu2017/bin/sysinfo
  - Rev: r5974 of 2011-05-13 9bcede8f2999c33d61f64985e45859ea9
  - running on linux      4.15-0.5 Fri Aug 23 19:05:07 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

[https://www.spec.org/cpu2017/Docs/config.html#sysinfo](https://www.spec.org/cpu2017/Docs/config.html#sysinfo)

- From /proc/cpuinfo
  - model name: Intel(R) Xeon(R) Platinum 8256 CPU @ 3.80GHz
  - 8 "physical id"s (chips)
  - 8 "processors"
  - cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    - cpu cores: 4
    - siblings: 4
    - physical 0: cores 1 2 4 13
    - physical 1: cores 1 2 12 13

- From /proc/cpuinfo
  - x86_64
  - 32-bit, 64-bit
  - Little Endian

---

**Non-Compliant**

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---

(Continued on next page)
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

On-line CPU(s) list: 0-7
Thread(s) per core: 1
Core(s) per socket: 4
Socket(s): 2
NUMA node(s): 2
Vendor ID: Intel(R)
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8256 CPU @ 3.80GHz
Stepping:
CPU MHz:
CPU max MHz: 3800.000
CPU min MHz: 1200.0000
BogoMIPS: 7600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 16896K
NUMA node0 CPU(s): 0-3
NUMA node1 CPU(s): 4-7
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
mdtes64 startup_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtrnr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
ekv cat_13 cdp_l3 invpcid_single intel_patin mba tpr_shadow vnni flexpriority ept
vld fsgsbase tsc_adjunct bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap cflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xsavec xsaveopt xsaveopt xsaveopt xsaveopt xsaveopt xsaveopt xsaveopt
/proc/cpuinfo cache data
cache size: 16896 KB

(Continued on next page)
Cisco Systems  
Cisco UCS C240 M5 (Intel Xeon Platinum 8256, 3.80GHz)

| SPECspeed®2017_fp_base =  |
| SPECspeed®2017_fp_peak =  |

| CPU2017 License: | 9019 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |
| Test Date: | Aug-2019 |
| Hardware Availability: | Apr-2019 |
| Software Availability: | May-2019 |

**SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.**

---

**Platform Notes (Continued)**

From `numactl --hardware` WARNING: a numactl `node` might or might not correspond to a physical chip.

| available: | 2 nodes (0-1) |
| node 0 cpus: | 0 1 2 3 |
| node 0 size: | 385606 MB |
| node 0 free: | 378147 MB |
| node 1 cpus: | 4 5 6 7 |
| node 1 size: | 387059 MB |
| node 1 free: | 386574 MB |

node distances:

<table>
<thead>
<tr>
<th>node</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0:</td>
<td>10</td>
<td>21</td>
</tr>
<tr>
<td>1:</td>
<td>21</td>
<td>10</td>
</tr>
</tbody>
</table>

From `/proc/meminfo`

| MemTotal: | 791209960 kB |
| HugePages_Total: | 0 |
| Hugepagesize: | 2048 kB |

From `/etc/*release* /etc/*version*`

| NAME= | SUSE Linux Enterprise Server 15 |
| VERSION= | "15" |
| VERSION_ID= | "15" |
| PRETTY_NAME= | "SUSE Linux Enterprise Server 15" |
| ID= | "sles" |
| ID_LIKE= | "suse" |
| ANSI_COLOR= | "0;32" |
| CPE_NAME= | "cpe:/o:suse:sles:15" |

uname -a:

Linux linux-4vt5 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)   x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected

(Continued on next page)
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Platform Notes (Continued)

CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 23 14:07

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 224G 26G 198G 12% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

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<tr>
<th>619.lbm_s(base, peak) 638.imagick_s(base, peak) 644.nab_s(base, peak)</th>
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</table>

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C, Fortran | 607.cactuBSSN_s(base, peak)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8256, 3.80GHz)

SPECSpeed®2017_fp_base = 
SPECSpeed®2017_fp_peak =

CPU2017 License: 9019
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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------------------
Fortran | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
         654.roms_s(base, peak)
------------------------------------------------------------------------------------------

------------------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------------------

------------------------------------------------------------------------------------------
Fortran, C | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
            628.pop2_s(base, peak)
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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------------------------------------------------------------------------------------------

------------------------------------------------------------------------------------------
Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

(Continued on next page)
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Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
   -assume bytetr
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
71.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

(Continued on next page)
**SPEC CPU®2017 Floating Point Speed Result**

Cisco Systems  
Cisco UCS C240 M5 (Intel Xeon Platinum 8256, 3.80GHz)  

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**Specifications**  
CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Aug-2019  
Hardware Availability: Apr-2019  
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**Base Optimization Flags (Continued)**

Benchmarks using both Fortran and C:  
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:  
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-nostandard-realloc-lhs

**Peak Compiler Invocation**

C benchmarks:  
icc -m64 -std=c11  

Fortran benchmarks:  
ifort -m64

Peak compiler using both Fortran and C:  
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:  
icpc -m64 icc -m64 -std=c11 ifort -m64

**Peak Portability Flags**

Same as Base Portability Flags
## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
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### Peak Optimization Flags

**C benchmarks:**
- `-xCORE-AVX512`  
- `-ipo -O3 -no-prec-div -qopt-prefetch`  
- `-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`

**Fortran benchmarks:**
- `603.bwaves_s`: `-prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP`  
- `-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3`  
- `-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4 -qopenmp -nstandard-realloc-lhs`

- `649.fotonik3d_s`: Same as `603.bwaves_s`

- `654.roms_s`: `-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div`  
  `-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -nstandard-realloc-lhs`

**Benchmarks using both Fortran and C:**
- `621.wrf_s`: `-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512`  
  `-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp`  
  `-DSPEC_OPENMP -nstandard-realloc-lhs`

- `628.pop2_s`: Same as `621.wrf_s`

**Benchmarks using Fortran, C, and C++:**
- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`  
- `-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`  
- `-nstandard-realloc-lhs`

---

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Non-Compliant
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The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

Non-Compliant