Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6246, 3.30GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

503.bwaves_r  48  132
507.caactuBSSN_r  48  132
508.namd_r  48  138
510.parest_r  48  125
511.povray_r  48  203
519.lbm_r  48  106
521.wrf_r  48  207
526.blender_r  48  192
527.cam4_r  48  209
538.imagick_r  48  213
544.nab_r  48  304
549.fotonik3d_r  48  209
554.roms_r  48  104

--- SPECrate®2017_fp_base (190)   --- SPECrate®2017_fp_peak (193)

CPU Name: Intel Xeon Gold 6246
Max MHz: 4200
Nominal: 3300
Enabled: 24 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 1.9 TB SSD SAS
Other: None

OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.3 released Mar-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: --
Cisco Systems
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>48</td>
<td>955</td>
<td>504</td>
<td>954</td>
<td>504</td>
<td>954</td>
<td>504</td>
<td>955</td>
<td>504</td>
<td>955</td>
<td>504</td>
<td>955</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>48</td>
<td>460</td>
<td>132</td>
<td>460</td>
<td>132</td>
<td>460</td>
<td>132</td>
<td>460</td>
<td>132</td>
<td>460</td>
<td>132</td>
<td>460</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>48</td>
<td>332</td>
<td>138</td>
<td>330</td>
<td>138</td>
<td>331</td>
<td>138</td>
<td>331</td>
<td>138</td>
<td>331</td>
<td>138</td>
<td>331</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>48</td>
<td>1001</td>
<td>125</td>
<td>1001</td>
<td>125</td>
<td>1001</td>
<td>125</td>
<td>1001</td>
<td>125</td>
<td>1001</td>
<td>125</td>
<td>1001</td>
</tr>
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<td>511.povray_r</td>
<td>48</td>
<td>553</td>
<td>203</td>
<td>554</td>
<td>202</td>
<td>552</td>
<td>203</td>
<td>552</td>
<td>203</td>
<td>552</td>
<td>203</td>
<td>552</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>48</td>
<td>479</td>
<td>106</td>
<td>480</td>
<td>105</td>
<td>479</td>
<td>106</td>
<td>479</td>
<td>106</td>
<td>479</td>
<td>106</td>
<td>479</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>48</td>
<td>517</td>
<td>208</td>
<td>519</td>
<td>207</td>
<td>519</td>
<td>207</td>
<td>519</td>
<td>207</td>
<td>519</td>
<td>207</td>
<td>519</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>48</td>
<td>380</td>
<td>192</td>
<td>381</td>
<td>192</td>
<td>382</td>
<td>192</td>
<td>382</td>
<td>192</td>
<td>382</td>
<td>192</td>
<td>382</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>48</td>
<td>402</td>
<td>209</td>
<td>403</td>
<td>208</td>
<td>402</td>
<td>209</td>
<td>402</td>
<td>209</td>
<td>402</td>
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<td>402</td>
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<tr>
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<td>48</td>
<td>272</td>
<td>438</td>
<td>273</td>
<td>438</td>
<td>273</td>
<td>438</td>
<td>273</td>
<td>438</td>
<td>273</td>
<td>438</td>
<td>273</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>48</td>
<td>268</td>
<td>302</td>
<td>266</td>
<td>304</td>
<td>265</td>
<td>305</td>
<td>264</td>
<td>306</td>
<td>264</td>
<td>306</td>
<td>264</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>48</td>
<td>1273</td>
<td>147</td>
<td>1273</td>
<td>147</td>
<td>1273</td>
<td>147</td>
<td>1273</td>
<td>147</td>
<td>1273</td>
<td>147</td>
<td>1273</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>48</td>
<td>729</td>
<td>105</td>
<td>732</td>
<td>104</td>
<td>732</td>
<td>104</td>
<td>733</td>
<td>104</td>
<td>735</td>
<td>104</td>
<td>735</td>
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</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
umactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6246, 3.30GHz)

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Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

---

General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

---

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-2vgg Fri Aug 30 20:25:24 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 12
siblings: 24
physical 0: cores 2 3 4 10 11 16 17 20 24 25 27
physical 1: cores 0 2 4 8 9 10 11 17 18 19 25 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz

(Continued on next page)
Cisco Systems
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CPU2017 License: 9019
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Platform Notes (Continued)

Stepping: 7
CPU MHz: 3300.000
CPU max MHz: 4200.0000
CPU min MHz: 1200.0000
BogoMIPS: 6600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0,1,6,7,9,10,24,25,30,31,33,34
NUMA node1 CPU(s): 2-5,8,11,26-29,32,35
NUMA node2 CPU(s): 12,13,15,16,19,22,36,37,39,40,43,46
NUMA node3 CPU(s): 14,17,18,20,21,23,38,41,42,44,45,47
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtsc64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdpl invpcid_single mba tpr_shadow vnmi flexpriority ept vpid fsgsbase
tsc_adjust bmi1 hle avx2 smep bmi2 ert msinvpcid rtm crq mpx rdt_a avx512f avx512dq
rsdoad adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 xsaves cqm_llc cqm_ocupp_llc cqm_mbm_total cqm_mbm_local ibpbb ibrs stibp
dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni
arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size : 25344 KB

From numactl --hardware WARNING: a numacl 'node' might or might not correspond to a
  physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 6 7 9 10 24 25 30 31 33 34
  node 0 size: 192075 MB
  node 0 free: 183030 MB
  node 1 cpus: 2 3 4 5 8 11 26 27 28 29 32 35
  node 1 size: 193528 MB
  node 1 free: 188063 MB
  node 2 cpus: 12 13 15 16 19 22 36 37 39 40 43 46
  node 2 size: 193528 MB
  node 2 free: 188053 MB
  node 3 cpus: 14 17 18 20 21 23 38 41 42 44 45 47
  node 3 size: 193526 MB
  node 3 free: 188028 MB
  node distances:
    node 0 1 2 3

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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6246, 3.30GHz) | SPECrate®2017_fp_base = 190
SPECrate®2017_fp_peak = 193

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### Platform Notes (Continued)

0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From `/proc/meminfo`
- MemTotal: 791202936 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release* /etc/*version*`
- os-release:
  - NAME="SLES"
  - VERSION="15"
  - VERSION_ID="15"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15"
  - ID="sles"
  - ID_LIKE="suse"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
- Linux linux-2vgg 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
- x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 30 13:33

SPEC is set to: /home/cpu2017
- Filesystem Type Size Used Avail Use% Mounted on
- /dev/sda1 xfs 373G 39G 335G 11% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
- BIOS Cisco Systems, Inc. C240M5.4.0.3.34.0301190218 03/01/2019
- Memory:
  - 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrater®2017_fp_base = 190
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Compiler Version Notes

-----------------------------------------------------------------
| C       | 519.lbm_r(base, peak) 538.imagick_r(base, peak) |
|         | 544.nab_r(base, peak) |
-----------------------------------------------------------------
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
-----------------------------------------------------------------

-----------------------------------------------------------------
| C++      | 508.namd_r(base, peak) 510.parest_r(base, peak) |
-----------------------------------------------------------------
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
-----------------------------------------------------------------

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| C++, C   | 511.povray_r(base, peak) 526.blender_r(base, peak) |
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| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
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| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
-----------------------------------------------------------------

-----------------------------------------------------------------
| C++, C, Fortran | 507.cactuBSSN_r(base, peak) |
-----------------------------------------------------------------
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
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| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
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| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
| Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
-----------------------------------------------------------------

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| Fortran   | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) |
|           | 554.roms_r(base, peak) |
-----------------------------------------------------------------
| Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) |
| (Continued on next page) |
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Compiler Version Notes (Continued)

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Fortran, C
521.wrf_r(base, peak) 527.cam4_r(base, peak)

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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
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519.lbm_r: -DSPEC_LP64

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### Base Portability Flags (Continued)

- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

### Base Optimization Flags

#### C benchmarks:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

#### C++ benchmarks:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

#### Fortran benchmarks:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

#### Benchmarks using both Fortran and C:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

#### Benchmarks using both C and C++:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

#### Benchmarks using Fortran, C, and C++:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

### Peak Compiler Invocation

#### C benchmarks:
- icc -m64 -std=c11

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Spec CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

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Peak Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags
C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

538.imagick_r: -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrater®2017_fp_base = 190
SPECrater®2017_fp_peak = 193

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Optimization Flags (Continued)

Fortran benchmarks:
503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
## SPEC CPU®2017 Floating Point Rate Result

### Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6246, 3.30GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>190</td>
<td>193</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Date:** Aug-2019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
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