Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6244, 3.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
CPU Name: Intel Xeon Gold 6244
Max MHz: 4400
Nominal: 3600
Enabled: 16 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4d released May-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: --

<table>
<thead>
<tr>
<th>Software</th>
<th>SPECrate®2017_fp_base = 149</th>
<th>SPECrate®2017_fp_peak = 151</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
</tr>
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<td>No</td>
<td></td>
</tr>
<tr>
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<td></td>
</tr>
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<td></td>
</tr>
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<td></td>
</tr>
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<td>64-bit</td>
<td></td>
</tr>
<tr>
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<td>64-bit</td>
<td></td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>Power Management</td>
<td>--</td>
<td></td>
</tr>
</tbody>
</table>

SPECrates

<table>
<thead>
<tr>
<th>Software</th>
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</tr>
</thead>
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<td></td>
</tr>
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<td></td>
</tr>
<tr>
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<td>--</td>
<td></td>
</tr>
</tbody>
</table>
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>32</td>
<td>693</td>
<td>463</td>
<td>690</td>
<td>465</td>
<td>690</td>
<td>465</td>
<td>32</td>
<td>691</td>
<td>465</td>
<td>702</td>
<td>457</td>
<td>694</td>
<td>463</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>32</td>
<td>433</td>
<td>93.6</td>
<td>432</td>
<td>93.7</td>
<td>432</td>
<td>93.7</td>
<td>32</td>
<td>433</td>
<td>93.5</td>
<td>433</td>
<td>93.6</td>
<td>434</td>
<td>93.4</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>32</td>
<td>305</td>
<td>99.6</td>
<td>305</td>
<td>99.7</td>
<td>305</td>
<td>99.7</td>
<td>32</td>
<td>303</td>
<td>100</td>
<td>304</td>
<td>100</td>
<td>305</td>
<td>99.6</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>32</td>
<td>794</td>
<td>105</td>
<td>795</td>
<td>105</td>
<td>797</td>
<td>105</td>
<td>32</td>
<td>796</td>
<td>105</td>
<td>796</td>
<td>105</td>
<td>800</td>
<td>105</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>32</td>
<td>502</td>
<td>149</td>
<td>504</td>
<td>148</td>
<td>502</td>
<td>149</td>
<td>32</td>
<td>432</td>
<td>173</td>
<td>429</td>
<td>174</td>
<td>430</td>
<td>174</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>32</td>
<td>384</td>
<td>87.8</td>
<td>385</td>
<td>87.7</td>
<td>384</td>
<td>87.8</td>
<td>32</td>
<td>384</td>
<td>87.7</td>
<td>385</td>
<td>87.6</td>
<td>385</td>
<td>87.7</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>32</td>
<td>413</td>
<td>174</td>
<td>406</td>
<td>176</td>
<td>402</td>
<td>178</td>
<td>32</td>
<td>390</td>
<td>184</td>
<td>403</td>
<td>178</td>
<td>394</td>
<td>182</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>32</td>
<td>357</td>
<td>137</td>
<td>358</td>
<td>136</td>
<td>357</td>
<td>136</td>
<td>32</td>
<td>356</td>
<td>137</td>
<td>357</td>
<td>137</td>
<td>357</td>
<td>136</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>32</td>
<td>366</td>
<td>153</td>
<td>364</td>
<td>154</td>
<td>364</td>
<td>154</td>
<td>32</td>
<td>362</td>
<td>155</td>
<td>360</td>
<td>156</td>
<td>355</td>
<td>158</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>32</td>
<td>247</td>
<td>218</td>
<td>246</td>
<td>219</td>
<td>246</td>
<td>219</td>
<td>32</td>
<td>246</td>
<td>219</td>
<td>247</td>
<td>218</td>
<td>247</td>
<td>218</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>32</td>
<td>1000</td>
<td>125</td>
<td>999</td>
<td>125</td>
<td>1001</td>
<td>125</td>
<td>32</td>
<td>1004</td>
<td>124</td>
<td>1009</td>
<td>124</td>
<td>1007</td>
<td>124</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>32</td>
<td>537</td>
<td>94.6</td>
<td>539</td>
<td>94.4</td>
<td>535</td>
<td>95.1</td>
<td>32</td>
<td>539</td>
<td>94.3</td>
<td>542</td>
<td>93.8</td>
<td>541</td>
<td>93.9</td>
</tr>
</tbody>
</table>

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**General Notes**

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
## SPEC CPU®2017 Floating Point Rate Result

### Cisco Systems

**Cisco UCS C240 M5 (Intel Xeon Gold 6244, 3.60GHz)**

<table>
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<tr>
<th>SPECrate®2017_fp_peak</th>
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</tr>
</thead>
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<td>151</td>
<td>149</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  

### General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

**BIOS Settings:**  
Intel HyperThreading Technology set to Enabled  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program `/home/cpu2017/bin/sysinfo`  
Rev: r5974 of 2018-05-19 9bced2f999c33d61f64985e45859ea9  
running on linux-uuav Fri Aug 16 22:20:39 2019

**SUT (System Under Test) info as seen by some common utilities.**  
For more information on this section, see  
[https://www.spec.org/cpu2017/Docs/config.html#sysinfo](https://www.spec.org/cpu2017/Docs/config.html#sysinfo)

```
From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 6244 CPU @ 3.60GHz
  2 "physical id"s (chips)
  32 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 8
  siblings : 16
  physical 0: cores 2 3 9 16 17 20 26 27
  physical 1: cores 1 2 8 9 19 20 26 27
```

```
From lscpu:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order: Little Endian
  CPU(s): 32
  On-line CPU(s) list: 0-31
  Thread(s) per core: 2
  Core(s) per socket: 8
  Socket(s): 2
  NUMA node(s): 4
  Vendor ID: GenuineIntel
  CPU family: 6
  Model: 85
  Model name: Intel(R) Xeon(R) Gold 6244 CPU @ 3.60GHz
  Stepping: 6
```

(Continued on next page)
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Tested by: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

| SPECrate®2017_fp_base = 149 |
| SPECrate®2017_fp_peak = 151 |

Platform Notes (Continued)

CPU MHz: 3600.000
CPU max MHz: 4400.0000
CPU min MHz: 1200.0000
BogoMIPS: 7200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0,2-4,16,18-20
NUMA node1 CPU(s): 1,5-7,17,21-23
NUMA node2 CPU(s): 8-11,24-27
NUMA node3 CPU(s): 12-15,28-31

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vmmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ibrm msrxbms rbxtsd dtc tsc
peek avx2 smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
genetic chip.

| available: 4 nodes (0-3) |
| node 0 cpus: 0 2 3 4 16 18 19 20 |
| node 0 size: 192104 MB |
| node 0 free: 184614 MB |
| node 1 cpus: 1 5 6 7 17 21 22 23 |
| node 1 size: 193529 MB |
| node 1 free: 189533 MB |
| node 2 cpus: 8 9 10 11 24 25 26 27 |
| node 2 size: 193529 MB |
| node 2 free: 189529 MB |
| node 3 cpus: 12 13 14 15 28 29 30 31 |
| node 3 size: 193498 MB |
| node 3 free: 189447 MB |

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Platform Notes (Continued)

1:  11  10  21  21
2:  21  21  10  11
3:  21  21  11  10

From /proc/meminfo
 MemTotal: 791205796 kB
 HugePages_Total: 0
 Hugepagesize: 2048 kB

From /etc/*release*, /etc/*version*
 os-release:
 NAME="SLES"
 VERSION="15"
 VERSION_ID="15"
 PRETTY_NAME="SUSE Linux Enterprise Server 15"
 ID="sles"
 ID_LIKE="suse"
 ANSI_COLOR="0;32"
 CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
 Linux linux-uuav 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
 x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 16 15:44

SPEC is set to: /home/cpu2017
 Filesystem Type Size Used Avail Use% Mounted on
 /dev/sda1 xfs 224G 37G 188G 17% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
 BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
 Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6244, 3.60GHz)

SPECrater®2017_fp_base = 149
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
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Compiler Version Notes

==============================================================================
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<thead>
<tr>
<th>C</th>
<th>519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) C</td>
<td>Intel(R) 64 Compiler for applications running on Intel(R) 64,</td>
</tr>
<tr>
<td></td>
<td>Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td>________________</td>
<td>---------------------------------------------------------------------</td>
</tr>
<tr>
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</tr>
<tr>
<td>-----------------</td>
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</tr>
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<td>-----------------</td>
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</tr>
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<td>C++, C, Fortran</td>
<td>507.cactuBSSN_r(base, peak)</td>
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</tr>
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</tr>
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<td>Intel(R) Fortran</td>
<td>Intel(R) 64 Compiler for applications running on Intel(R) 64,</td>
</tr>
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<td></td>
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</tr>
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<td>Intel(R) 64 Compiler for applications running on Intel(R)</td>
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</table>
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**Compiler Version Notes (Continued)**

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Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran, C
521.wrf_r(base, peak) 527.cam4_r(base, peak)

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64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

**Base Compiler Invocation**

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

**Base Portability Flags**

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
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<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Aug-2019</td>
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<td>Apr-2019</td>
</tr>
<tr>
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<td>May-2019</td>
</tr>
</tbody>
</table>

**Base Portability Flags (Continued)**

521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

**Peak Compiler Invocation**

C benchmarks:
icc -m64 -std=c11

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6244, 3.60GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 149</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 151</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
544.nab_r: Same as 538.imagick_r

C++ benchmarks:
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6244, 3.60GHz)

SPECratenew $\text{SPECrate}^{\text{new}}_{2017 \text{fp base}} = 149$
SPECratenew $\text{SPECrate}^{\text{new}}_{2017 \text{fp peak}} = 151$

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
# SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 6244, 3.60GHz)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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