## SPEC CPU®2017 Integer Rate Result

### Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4208, 2.10GHz)

| Test Date: | Sep-2019 |
| Test Sponsor: | Cisco Systems |
| CPU2017 License: | 9019 |
| Tested by: | Cisco Systems |
| Hardware Availability: | Apr-2019 |
| Software Availability: | May-2019 |

### SPECrate®2017_int_base = 84.5
SPECrate®2017_int_peak = Not Run

### Hardware
- **CPU Name:** Intel Xeon Silver 4208
- **Max MHz:** 3200
- **Nominal:** 2100
- **Enabled:** 16 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 11 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 15 (x64_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4d released May-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --

### Results

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>84.5</th>
</tr>
</thead>
</table>

### Test Conditions

<table>
<thead>
<tr>
<th>Test</th>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_r</td>
<td>32</td>
<td>63.0</td>
<td>Not Run</td>
</tr>
<tr>
<td>gcc_r</td>
<td>32</td>
<td>72.2</td>
<td></td>
</tr>
<tr>
<td>mcf_r</td>
<td>32</td>
<td>58.8</td>
<td></td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>32</td>
<td>103</td>
<td></td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>32</td>
<td>148</td>
<td></td>
</tr>
<tr>
<td>x264_r</td>
<td>32</td>
<td>148</td>
<td></td>
</tr>
<tr>
<td>deepsjeng_r</td>
<td>32</td>
<td>68.4</td>
<td></td>
</tr>
<tr>
<td>leela_r</td>
<td>32</td>
<td>103</td>
<td></td>
</tr>
<tr>
<td>exchange2_r</td>
<td>32</td>
<td>164</td>
<td></td>
</tr>
<tr>
<td>mcf_r</td>
<td>32</td>
<td>56.1</td>
<td></td>
</tr>
<tr>
<td>xz_r</td>
<td>32</td>
<td>56.1</td>
<td></td>
</tr>
</tbody>
</table>

---

Page 1

Standard Performance Evaluation Corporation (info@spec.org)  https://www.spec.org/
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4208, 2.10GHz)

SPEC®2017_int_base = 84.5
SPEC®2017_int_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>32</td>
<td>806</td>
<td>63.2</td>
<td>813</td>
<td>62.7</td>
<td>809</td>
<td>63.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>32</td>
<td>625</td>
<td>72.5</td>
<td>628</td>
<td>72.1</td>
<td>628</td>
<td>72.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>32</td>
<td>446</td>
<td>116</td>
<td>443</td>
<td>117</td>
<td>443</td>
<td>117</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>32</td>
<td>713</td>
<td>58.9</td>
<td>714</td>
<td>58.8</td>
<td>715</td>
<td>58.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>32</td>
<td>330</td>
<td>102</td>
<td>329</td>
<td>103</td>
<td>330</td>
<td>103</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>525.x264_r</td>
<td>32</td>
<td>377</td>
<td>149</td>
<td>379</td>
<td>148</td>
<td>378</td>
<td>148</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>32</td>
<td>537</td>
<td>68.3</td>
<td>536</td>
<td>68.4</td>
<td>536</td>
<td>68.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>541.leela_r</td>
<td>32</td>
<td>847</td>
<td>62.5</td>
<td>854</td>
<td>62.1</td>
<td>853</td>
<td>62.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>32</td>
<td>511</td>
<td>164</td>
<td>512</td>
<td>164</td>
<td>511</td>
<td>164</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>32</td>
<td>616</td>
<td>56.1</td>
<td>616</td>
<td>56.1</td>
<td>616</td>
<td>56.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SPEC®2017_int_base = 84.5
SPEC®2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
umactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4208, 2.10GHz)

SPECrate®2017_int_base = 84.5
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-3c6s Mon Sep 2 09:16:34 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
  2 "physical id"s (chips)
  32 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 8
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order: Little Endian
  CPU(s): 32
  On-line CPU(s) list: 0-31
  Thread(s) per core: 2
  Core(s) per socket: 8
  Socket(s): 2
  NUMA node(s): 2
  Vendor ID: GenuineIntel
  CPU family: 6
  Model: 85
  Model name: Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
  Stepping: 6
  CPU MHz: 2100.000
  CPU max MHz: 3200.0000
  CPU min MHz: 800.0000

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4208, 2.10GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

**SPECr®2017_int_base** = 84.5

**SPECr®2017_int_peak** = Not Run

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Sep-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Avail:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Avail:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

- **BogoMIPS:** 4200.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 11264K
- **NUMA node0 CPU(s):** 0-7,16-23
- **NUMA node1 CPU(s):** 8-15,24-31
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
- **/proc/cpuinfo cache data**
  - cache size: 11264 KB
- **From numactl --hardware** WARNING: a numactl 'node' might or might not correspond to a physical chip.
  - available: 2 nodes (0-1)
  - node 0 cpus: 0 1 2 3 4 5 6 7 16 18 19 20 21 22 23
  - node 0 size: 385604 MB
  - node 0 free: 385037 MB
  - node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
  - node 1 size: 387056 MB
  - node 1 free: 386573 MB
  - node distances:
    - node 0 1
      - 0: 10 21
      - 1: 21 10

**From /proc/meminfo**
- MemTotal: 791205404 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

**From /etc/*release* /etc/*version**
- os-release:
  - NAME="SLES"
  - VERSION="15"

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4208, 2.10GHz)  

SPECrater®2017_int_base =  
84.5

SPECrater®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-3c6s 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 2 09:16

SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda1      xfs   224G   20G  204G   9% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

--------------------------------------------------------------------------------------------------------------------------
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)  
| 525.x264_r(base) 557.xz_r(base)
--------------------------------------------------------------------------------------------------------------------------

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------------------------------------------------

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4208, 2.10GHz)

| SPECrate®2017_int_base = 84.5 |
| SPECrate®2017_int_peak = Not Run |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

| Test Date: Sep-2019 |
| Hardware Availability: Apr-2019 |
| Software Availability: May-2019 |

### Compiler Version Notes (Continued)

#### C++
- 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) 541.leela_r(base)

---

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

#### Fortran
- 548.exchange2_r(base)

---

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

### Base Compiler Invocation

- **C benchmarks:**
  
  ```
  icc -m64 -std=c11
  ```

- **C++ benchmarks:**
  
  ```
  icpc -m64
  ```

- **Fortran benchmarks:**
  
  ```
  ifort -m64
  ```

### Base Portability Flags

- 500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
- 502.gcc_r: -DSPEC_LP64
- 505.mcf_r: -DSPEC_LP64
- 520.omnetpp_r: -DSPEC_LP64
- 523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
- 525.x264_r: -DSPEC_LP64
- 531.deepsjeng_r: -DSPEC_LP64
- 541.leela_r: -DSPEC_LP64
- 548.exchange2_r: -DSPEC_LP64
- 557.xz_r: -DSPEC_LP64
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4208, 2.10GHz)

SPECratenos_run
SPECratenos_run

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Date</th>
<th>Test Sponsor</th>
<th>Hardware Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>9019</td>
<td>Sep-2019</td>
<td>Cisco Systems</td>
<td>Apr-2019</td>
</tr>
</tbody>
</table>

Tested by: Cisco Systems
Software Availability: May-2019

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

SPEC CPU and SPECratenos_run are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product
names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-09-01 23:46:34-0400.
Originally published on 2019-10-01.