## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4208, 2.10GHz)

**SPECrater®2017_int_base = 84.5**

**SPECrater®2017_int_peak = Not Run**

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Sep-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Silver 4208
- **Max MHz:** 3200
- **Nominal:** 2100
- **Enabled:** 16 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 11 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x64_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4d released May-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --

---

Copy of the SPEC CPU®2017 Integer Rate Result test results for Cisco UCS C240 M5 (Intel Xeon Silver 4208, 2.10GHz) showing SPECrate®2017_int_base = 84.5 and SPECrate®2017_int_peak = Not Run. The test was performed by Cisco Systems on Sep-2019, with software availability on May-2019.
## SPEC CPU®2017 Integer Rate Result

### Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4208, 2.10GHz)

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Sep-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>32</td>
<td>806</td>
<td>63.2</td>
<td>813</td>
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<td>502.gcc_r</td>
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<td>72.5</td>
<td>628</td>
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<td>505.mcf_r</td>
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<td>443</td>
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<td>443</td>
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<td>58.8</td>
<td>715</td>
<td>58.7</td>
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<td>523.xalancbmk_r</td>
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<td>102</td>
<td>329</td>
<td>103</td>
<td>330</td>
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<td>525.x264_r</td>
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<tr>
<td>531.deepsjeng_r</td>
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<td>541.leela_r</td>
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<td>548.exchange2_r</td>
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<td>164</td>
<td>512</td>
<td>164</td>
<td>511</td>
<td>164</td>
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<tr>
<td>557.xz_r</td>
<td>32</td>
<td>616</td>
<td>56.1</td>
<td>616</td>
<td>56.1</td>
<td>616</td>
<td>56.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:  
`LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"`

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
`sync; echo 3> /proc/sys/vm/drop_caches`  
runcpu command invoked through numactl i.e.:  
`numactl --interleave=all runcpu <etc>`

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4208, 2.10GHz)

SPECratenew_int_base = 84.5
SPECratenew_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000
CPU max MHz: 3200.0000
CPU min MHz: 800.0000

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

### Platform Notes (Continued)

<table>
<thead>
<tr>
<th>Platform Notes</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>BogoMIPS</td>
<td>4200.00</td>
</tr>
<tr>
<td>L1d cache</td>
<td>32K</td>
</tr>
<tr>
<td>L1i cache</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache</td>
<td>1024K</td>
</tr>
<tr>
<td>L3 cache</td>
<td>11264K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s)</td>
<td>0-7,16-23</td>
</tr>
<tr>
<td>NUMA node1 CPU(s)</td>
<td>8-15,24-31</td>
</tr>
<tr>
<td>Flags</td>
<td>fpu vme de pse tsc msr mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscalls nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdpl_l3 invpcid_single intel_pinn mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cmx mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xsaveopt xgetbv1 xsavees cmx_llc cmx_occup_llc cmx_mb_total cmx_mb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd</td>
</tr>
<tr>
<td>/proc/cpuinfo cache data</td>
<td>cache size : 11264 KB</td>
</tr>
<tr>
<td>/proc/meminfo</td>
<td>MemTotal: 791205404 kB</td>
</tr>
<tr>
<td></td>
<td>HugePages_Total: 0</td>
</tr>
<tr>
<td></td>
<td>Hugepagesize: 2048 kB</td>
</tr>
</tbody>
</table>

(Continued on next page)
Platform Notes (Continued)

VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-3c6s 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

runtime 3 Sep 2 09:16

SPEC is set to: /home/cpu2017
    Filesystem     Type  Size  Used Avail Use% Mounted on
    /dev/sda1      xfs  224G   20G  204G  9% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base) 557.xz_r(base) |
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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**Compiler Version Notes (Continued)**

```plaintext
C++     | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) 541.leela_r(base)
```

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

```plaintext
Fortran | 548.exchange2_r(base)
```

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

**Base Compiler Invocation**

C benchmarks:
```sh
icc -m64 -std=c11
```

C++ benchmarks:
```sh
icpc -m64
```

Fortran benchmarks:
```sh
ifort -m64
```

**Base Portability Flags**

```plaintext
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```
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Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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