# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4210, 2.20GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Sep-2019</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### SPECrate®2017_int_base = 112

### SPECrate®2017_int_peak = Not Run

### Hardware

- **CPU Name:** Intel Xeon Silver 4210
- **Max MHz:** 3200
- **Nominal:** 2200
- **Enabled:** 20 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 13.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-25.25-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4c released Apr-2019
- **File System:** xfs
- **System State:** Run level 5 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --

### Table

<table>
<thead>
<tr>
<th>Test</th>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>40</td>
<td>84.2</td>
<td>Not Run</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>40</td>
<td>92.3</td>
<td>153</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>40</td>
<td>75.3</td>
<td>131</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>40</td>
<td>153</td>
<td>209</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>40</td>
<td>84.2</td>
<td>222</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>40</td>
<td>91.7</td>
<td>222</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>40</td>
<td>83.5</td>
<td>222</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>40</td>
<td>73.3</td>
<td>222</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>40</td>
<td>73.3</td>
<td>222</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>40</td>
<td>73.3</td>
<td>222</td>
</tr>
</tbody>
</table>

---

Copyright 2017-2020 Standard Performance Evaluation Corporation
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4210, 2.20GHz)

SPECrate®2017_int_base = 112
SPECrate®2017_int_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>40</td>
<td>757</td>
<td>84.1</td>
<td>755</td>
<td>84.3</td>
<td>756</td>
<td>84.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>40</td>
<td>613</td>
<td>92.4</td>
<td>614</td>
<td>92.3</td>
<td>617</td>
<td>91.8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>40</td>
<td>424</td>
<td>153</td>
<td>423</td>
<td>153</td>
<td>424</td>
<td>152</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>40</td>
<td>696</td>
<td>75.4</td>
<td>697</td>
<td>75.3</td>
<td>698</td>
<td>75.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>40</td>
<td>322</td>
<td>131</td>
<td>322</td>
<td>131</td>
<td>323</td>
<td>131</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>525.x264_r</td>
<td>40</td>
<td>335</td>
<td>209</td>
<td>336</td>
<td>208</td>
<td>336</td>
<td>209</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>40</td>
<td>500</td>
<td>91.6</td>
<td>500</td>
<td>91.7</td>
<td>500</td>
<td>91.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>541.leela_r</td>
<td>40</td>
<td>794</td>
<td>83.5</td>
<td>794</td>
<td>83.4</td>
<td>775</td>
<td>85.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>40</td>
<td>473</td>
<td>222</td>
<td>473</td>
<td>222</td>
<td>473</td>
<td>222</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>40</td>
<td>589</td>
<td>73.3</td>
<td>589</td>
<td>73.4</td>
<td>589</td>
<td>73.3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4210, 2.20GHz)

SPECrater®2017_int_base = 112
SPECrater®2017_int_peak = Not Run

General Notes (Continued)

is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-17bx Fri Sep 6 01:07:22 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
Stepping: 6
CPU MHz: 2200.000
CPU max MHz: 3200.0000
CPU min MHz: 1000.0000

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4210, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9,20-29
NUMA node1 CPU(s): 10-19,30-39
Flags:

From /proc/cpuinfo cache data
    cache size : 140800 KB

From numactl --hardware
    WARNING: a numactl 'node' might or might not correspond to a physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
    node 0 size: 385542 MB
    node 0 free: 384675 MB
    node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
    node 1 size: 386857 MB
    node 1 free: 386147 MB
    node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
    MemTotal: 790937540 kB
    HugePages_Total: 0
    Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
    os-release:
        NAME="SLES"
        VERSION="15"

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4210, 2.20GHz)

SPECrates®
SPECrates®
SPECrates®

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Platform Notes (Continued)

VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown):          Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 5 Sep 6 01:04

SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda3      xfs   324G   41G  283G  13% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.4c.0.0411190411 04/11/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th></th>
<th>500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>525.x264_r(base) 557.xz_r(base)</td>
</tr>
</tbody>
</table>
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4210, 2.20GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base =</th>
<th>112</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak =</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

### Compiler Version Notes (Continued)

<table>
<thead>
<tr>
<th>C++</th>
<th>520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) 541.leela_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fortran</th>
<th>548.exchange2_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

### Base Compiler Invocation

C benchmarks:
```bash
icc -m64 -std=c11
```

C++ benchmarks:
```bash
icpc -m64
```

Fortran benchmarks:
```bash
ifort -m64
```

### Base Portability Flags

- 500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
- 502.gcc_r: -DSPEC_LP64
- 505.mcf_r: -DSPEC_LP64
- 520.omnetpp_r: -DSPEC_LP64
- 523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
- 525.x264_r: -DSPEC_LP64
- 531.deepsjeng_r: -DSPEC_LP64
- 541.leela_r: -DSPEC_LP64
- 548.exchange2_r: -DSPEC_LP64
- 557.xz_r: -DSPEC_LP64
### Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4210, 2.20GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>112</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Sep-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

#### Base Optimization Flags

**C benchmarks:**
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
- `-lqkmalloc`

**C++ benchmarks:**
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
- `-lqkmalloc`

**Fortran benchmarks:**
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
- `-lqkmalloc`

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

---

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-09-06 04:07:22-0400.
Originally published on 2019-10-01.