Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrater®2017_int_base = 181
SPECrater®2017_int_peak = 187

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

500.perlbench_r 48
502.gcc_r 48
505.mcf_r 48
520.omnetpp_r 48
523.xalancbmk_r 48
525.x264_r 48
531.deepsjeng_r 48
541.leela_r 48
548.exchange2_r 48
557.xz_r 48

Hardware
CPU Name: Intel Xeon Gold 6246
Max MHz: 4200
Nominal: 3300
Enabled: 24 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 240G SSD SATA
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4g released Jul-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: --
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6246, 3.30GHz)

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Results Table

<table>
<thead>
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<td>114</td>
<td>454</td>
<td>114</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems
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SPEC CPU®2017 Integer Rate Result

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Software Availability: May-2019

General Notes (Continued)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bde8f2999c33d61f64985e4585ea9
running on linux-cud8 Thu Sep 12 10:35:41 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 24
physical 0: cores 0 2 4 8 9 10 11 17 18 19 25 27
physical 1: cores 1 2 3 4 10 11 16 17 20 24 25 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz
Stepping: 7

(Continued on next page)
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Platform Notes (Continued)

CPU MHz: 3300.000
CPU max MHz: 4200.0000
CPU min MHz: 1200.0000
BogoMIPS: 6600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0,1,3,4,7,10,24,25,27,28,31,34
NUMA node1 CPU(s): 2,5,6,8,9,11,26,29,30,32,33,35
NUMA node2 CPU(s): 12,13,18,19,21,22,36,37,42,43,45,46
NUMA node3 CPU(s): 14-17,20,23,38-41,44,47

Flags: fpu vme de pse tsc msr pae mce cmovpat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_ppnin mba tpr_shadow vmmvx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rdviat_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xsavec xnvmsog qcm_lccc qcm_occur_lccc qcm_mbb_total qcm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_prg_req pku osppe avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 1 3 4 7 10 24 25 27 28 31 34
node 0 size: 192120 MB
node 0 free: 191711 MB
node 1 cpus: 2 5 6 8 9 11 26 29 30 32 33 35
node 1 size: 193528 MB
node 1 free: 193195 MB
node 2 cpus: 12 13 18 19 21 22 36 37 42 43 45 46
node 2 size: 193499 MB
node 2 free: 193277 MB
node 3 cpus: 14 15 16 17 20 23 38 39 40 41 44 47
node 3 size: 193526 MB
node 3 free: 193299 MB
node distances:

0: 10 11 21 21

(Continued on next page)
Cisco Systems
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SPEC CPU®2017 Integer Rate Result
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SPECratenav<sub>2017_int_base</sub> = 181
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CPU2017 License: 9019
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Test Date: Sep-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo

MemTotal: 791219408 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-cud8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 12 07:44

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 224G 19G 205G 9% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
## SPEC CPU®2017 Integer Rate Result

### Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6246, 3.30GHz)

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**SPECrate®2017_int_base = 181**

**SPECrate®2017_int_peak = 187**

### Compiler Version Notes

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<tr>
<th>Platform</th>
<th>Compiler</th>
<th>Notes</th>
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<tbody>
<tr>
<td>C</td>
<td>502.gcc_r(peak)</td>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416 Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td></td>
<td>500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)</td>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>C++</td>
<td>523.xalancbmk_r(peak)</td>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416 Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
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Compiler Version Notes (Continued)
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C++ | 523.xalancbmk_r(peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

Base Compiler Invocation
C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

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SPEC CPU®2017 Integer Rate Result
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Base Portability Flags (Continued)

502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

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Fortran benchmarks:
ifort -m64

Peak Compiler Invocation (Continued)

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

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**SPEC CPU®2017 Integer Rate Result**

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### Peak Optimization Flags (Continued)

#### C++ benchmarks:

- `523.xalancbmk_r`: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib -ljemalloc`
- `531.deepsjeng_r`: Same as `520.omnetpp_r`
- `541.leela_r`: Same as `520.omnetpp_r`

#### Fortran benchmarks:


The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


---

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-09-12 13:35:41-0400.
Report generated on 2020-12-15 17:57:05 by CPU2017 PDF formatter v6255.
Originally published on 2019-10-01.