## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

**SPECrate®2017_fp_base = 247**

**SPECrate®2017_fp_peak = 250**

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Gold 6252N</td>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
</tr>
<tr>
<td>Max MHz: 3600</td>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Nominal: 2300</td>
<td>Parallel: No</td>
</tr>
<tr>
<td>Enabled: 48 cores, 2 chips, 2 threads/core</td>
<td>Firmware: Version 4.0.4c released Apr-2019</td>
</tr>
<tr>
<td>Orderable: 1,2 Chips</td>
<td>File System: xfs</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>L2: 1 MB I+D on chip per core</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>L3: 35.75 MB I+D on chip per core</td>
<td>Peak Pointers: 64-bit</td>
</tr>
<tr>
<td>Other: None</td>
<td>Other: None</td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)</td>
<td>Power Management: --</td>
</tr>
<tr>
<td>Storage: 1 x 1.9 TB SSD SAS</td>
<td></td>
</tr>
</tbody>
</table>

### Test Details

- **CPU2017 License:** 9019
- **Test Sponsor:** Cisco Systems
- **Test by:** Cisco Systems
- **Hardware Availability:** Apr-2019
- **Software Availability:** May-2019
- **Test Date:** Sep-2019
- **Tested by:** Cisco Systems
- **Test Sponsor:** Cisco Systems
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>503.bwaves_r</td>
<td>96</td>
<td>1788</td>
<td>538</td>
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<tr>
<td>507.cactuBSSN_r</td>
<td>96</td>
<td>585</td>
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<td>508.namd_r</td>
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<td>510.parest_r</td>
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<td>519.ibm_r</td>
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<td>544.nab_r</td>
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<td>549.fotonik3d_r</td>
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<td>554.roms_r</td>
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<td>106</td>
<td>1431</td>
<td>107</td>
<td>1437</td>
<td>106</td>
</tr>
</tbody>
</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3>/proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

SPECrate®2017_fp_base = 247
SPECrate®2017_fp_peak = 250

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bce8f2999c33d61f64985e45859ea9
running on linux-4z0x Sat Sep 14 21:27:06 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Gold 6252N CPU @ 2.30GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 24
  siblings: 48
  physical 0: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
  physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6252N CPU @ 2.30GHz

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

**SPEC CPU®2017 Floating Point Rate Result**

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Sep-2019  
**CPU MHz:** 2300.000  
**CPU max MHz:** 3600.0000  
**CPU min MHz:** 1000.0000  
**BogoMIPS:** 4600.00  
**Virtualization:** VT-x  
**L1d cache:** 32K  
**L1i cache:** 32K  
**L2 cache:** 1024K  
**L3 cache:** 36608K  
**NUMA node0 CPU(s):** 0-3,7,8,12-14,18-20,48-50,55,56,60-62,66-68  
**NUMA node1 CPU(s):** 4-6,9-11,15-17,21-23,52-54,57-59,63-65,69-71  
**NUMA node2 CPU(s):** 24-27,31-33,37-39,43,44,72-75,79-81,85-87,91,92  
**NUMA node3 CPU(s):** 28-30,34-36,40-42,45-47,76-78,82-84,88-90,93-95  
**Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp lm constant_tcb art arch_perfmon pebs bts rep_good nop1 xtopology nonstop_tcb cpuid aperfmperrf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrm pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pproc mba tpr_shadow vmmi flexpriority ept vpid fsxsbased tsc_adjust bni1 hle avx2 smep bmi2 erms invpcid rdtd_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsave xgetbv1 xsaves cqm_llc cqm_occum_llc cqm_mmb_total cqm_mmb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
   cache size : 36608 KB

From numactl --hardware  
WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 4 nodes (0-3)
   node 0 cpus: 0 1 2 3 7 8 12 13 14 18 19 20 48 49 50 51 55 56 60 61 62 66 67 68
   node 0 size: 192101 MB
   node 0 free: 178471 MB
   node 1 cpus: 4 5 6 9 10 11 15 16 17 21 22 23 52 53 54 57 58 59 63 64 65 69 70 71
   node 1 size: 193497 MB
   node 1 free: 183497 MB
   node 2 cpus: 24 25 26 27 31 32 33 37 38 39 43 44 72 73 74 75 79 80 81 85 86 87 91 92
   node 2 size: 193526 MB
   node 2 free: 183580 MB
   node 3 cpus: 28 29 30 34 35 36 40 41 42 45 46 47 76 77 78 82 83 84 88 89 90 93 94 95
   node 3 size: 193523 MB
   node 3 free: 183584 MB
   node distances:
      node 0 1 2 3

---

**SPECrate®2017_fp_base = 247**  
**SPECrate®2017_fp_peak = 250**

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(Continued on next page)
## Platform Notes (Continued)

0:  10  11  21  21  
1:  11  10  21  21  
2:  21  21  10  11  
3:  21  21  11  10  

From `/proc/meminfo`
- MemTotal: 791191776 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release* /etc/*version*`
```bash
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

uname -a:
```
Linux linux-4z0x 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBBP, IBRS_FW

run-level 3 Sep 14 12:42

SPEC is set to: /home/cpu2017
```bash
Filesystem  Type  Size  Used Avail Use% Mounted on
/dev/sda1   xfs  891G  70G  821G  8% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
- BIOS Cisco Systems, Inc. C240M5.4.0.4c.0.0411190411 04/11/2019
- Memory: 24x 0xce00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Sep-2019</td>
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<td>Hardware Availability:</td>
<td>Apr-2019</td>
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<tr>
<td>Software Availability:</td>
<td>May-2019</td>
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**Compiler Version Notes**

<table>
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<tr>
<th>Compiler</th>
<th>Version Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)</td>
</tr>
<tr>
<td></td>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>C++</td>
<td>508.namd_r(base, peak) 510.parest_r(base, peak)</td>
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<tr>
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<td>C++, C</td>
<td>511.povray_r(base, peak) 526.blender_r(base, peak)</td>
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<tr>
<td>C++, C, Fortran</td>
<td>507.cactuBSSN_r(base, peak)</td>
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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

Spec CPU®2017 Floating Point Rate Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

SPECrate®2017_fp_base = 247
SPECrate®2017_fp_peak = 250

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
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Compiler Version Notes (Continued)

64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
----------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64

(Continued on next page)
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| SPECrate®2017_fp_base = 247 |
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CPU2017 License: 9019
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Base Portability Flags (Continued)

521. wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526. blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527. cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538. imagick_r: -DSPEC_LP64
544. nab_r: -DSPEC_LP64
549. fotonik3d_r: -DSPEC_LP64
554. roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)  
SPECrater®2017_fp_base = 247
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Compiler Invocation (Continued)

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64

Benchmarks using both Fortran and C:
  ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
  icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
  icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
  519.lbm_r -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
  538.imagick_r -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
  544.nab_r: Same as 538.imagick_r

C++ benchmarks:
  508.namd_r -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
  510.parest_r -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
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Peak Optimization Flags (Continued)

Fortran benchmarks:
503.bwaves_r:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:
511.povray_r:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

526.blender_r:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:
<table>
<thead>
<tr>
<th>Cisco Systems</th>
<th>SPECrate\textsuperscript{®}2017_fp_base = 247</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cisco UCSC240 M5 (Intel Xeon Gold 6252N, 2.30GHz)</td>
<td>SPECrate\textsuperscript{®}2017_fp_peak = 250</td>
</tr>
</tbody>
</table>

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Software Availability: May-2019

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