Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 5220S, 2.70GHz)

<table>
<thead>
<tr>
<th>Test Sponsor</th>
<th>Cisco Systems</th>
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<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>CPU2017 License</td>
<td>9019</td>
</tr>
<tr>
<td>CPU Name</td>
<td>Intel Xeon Gold 5220S</td>
</tr>
<tr>
<td>Max MHz</td>
<td>3900</td>
</tr>
<tr>
<td>Nominal</td>
<td>2700</td>
</tr>
<tr>
<td>Enabled</td>
<td>36 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3:</td>
<td>24.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other:</td>
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</tr>
<tr>
<td>Memory:</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)</td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 1.9 TB SSD SAS</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>OS:</td>
<td>SUSE Linux Enterprise Server 15 (x86_64)</td>
</tr>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
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<tr>
<td>Firmware:</td>
<td>Version 4.0.4c released Apr-2019</td>
</tr>
<tr>
<td>File System:</td>
<td>xfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 5 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other:</td>
<td>jemalloc memory allocator V5.0.1</td>
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<td>Power Management:</td>
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SPECrated®2017_int_base = 204

SPECrated®2017_int_peak = 212

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Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

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<tr>
<td>502.gcc_r 72</td>
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</tr>
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<td>505.mcf_r 72</td>
<td>138</td>
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</tr>
<tr>
<td>520.omnetpp_r 72</td>
<td>229</td>
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</tr>
<tr>
<td>523.xalancbmk_r 72</td>
<td>248</td>
<td>405</td>
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<tr>
<td>525.x264_r 72</td>
<td>423</td>
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<tr>
<td>531.deepsjeng_r 72</td>
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<tr>
<td>541.leela_r 72</td>
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<tr>
<td>548.exchange2_r 72</td>
<td>401</td>
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<tr>
<td>557.xz_r 72</td>
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## Results Table

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<tr>
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<td>72</td>
<td>577</td>
<td>135</td>
<td>577</td>
<td>135</td>
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</tr>
</tbody>
</table>

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**General Notes**

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
```

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
umactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5220S, 2.70GHz)

SPEC CPU®2017 Integer Rate Result

| SPECrate®2017_int_base | = 204 |
| SPECrate®2017_int_peak | = 212 |

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Test Date: Sep-2019  
Tested by: Cisco Systems  
Hardware Availability: Apr-2019  
Software Availability: May-2019

General Notes (Continued)

is mitigated in the system as tested and documented.  
jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9  
running on linux-17bx Sat Sep 14 23:51:48 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 5220S CPU @ 2.70GHz
  2 "physical id"s (chips)
  72 "processors"
core, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
  siblings : 36
  physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
```

From lscpu:

```
Architecture:         x86_64
CPU op-mode(s):       32-bit, 64-bit
Byte Order:           Little Endian
CPU(s):               72
On-line CPU(s) list:  0-71
Thread(s) per core:   2
Core(s) per socket:   18
Socket(s):            2
NUMA node(s):         4
Vendor ID:            GenuineIntel
CPU family:           6
Model:                85
Model name:           Intel(R) Xeon(R) Gold 5220S CPU @ 2.70GHz
Stepping:             7
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5220S, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECrate&lt;sup&gt;®&lt;/sup&gt;2017_int_base</th>
<th>SPECrate&lt;sup&gt;®&lt;/sup&gt;2017_int_peak</th>
</tr>
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<tr>
<td>204</td>
<td>212</td>
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</tbody>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Sep-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

**Platform Notes (Continued)**

- **CPU MHz:** 2700.000  
- **CPU max MHz:** 3900.0000  
- **CPU min MHz:** 1000.0000  
- **BogoMIPS:** 5400.00  
- **Virtualization:** VT-x  
- **L1d cache:** 32K  
- **L1i cache:** 32K  
- **L2 cache:** 1024K  
- **L3 cache:** 25344K  
- **NUMA node0 CPU(s):** 0, 1, 2, 5, 6, 9, 10, 14, 15, 16, 17, 39, 40, 43, 44, 47, 49, 52, 53  
- **NUMA node1 CPU(s):** 3, 4, 7, 8, 11-13, 16, 17, 18, 19, 20, 23, 24, 27, 28, 32, 33, 54-56, 59, 60, 63, 64, 68, 69  
- **NUMA node2 CPU(s):** 21, 22, 25, 26, 29-31, 34, 35, 37, 38-40, 41, 42, 45, 46, 47, 49, 50, 51  
- **NUMA node3 CPU(s):** 21, 22, 25, 26, 29-31, 34, 35, 37, 38-40, 41, 42, 45, 46, 47, 49, 50, 51  
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm ablp_lm ablp_64fms ablp_lm ablp_64fms ablp_lm ablp_64fms ablp_lm ablp_64fms  

From numactl --hardware  
**Warning:** a numactl 'node' might or might not correspond to a physical chip. 
- **available:** 4 nodes (0-3)  
  - **node 0 cpus:** 0, 1, 2, 5, 6, 9, 10, 14, 15, 16, 17, 39, 40, 43, 44, 47, 48, 49, 52, 53  
  - **node 1 cpus:** 3, 4, 7, 8, 11, 12, 13, 16, 17, 39, 40, 43, 44, 47, 48, 49, 52, 53  
  - **node 2 cpus:** 18, 19, 20, 23, 24, 27, 28, 32, 33, 54, 55, 56, 59, 60, 63, 64, 68, 69  
  - **node 3 cpus:** 21, 22, 25, 26, 29, 30, 31, 34, 35, 37, 58, 61, 62, 65, 66, 67, 70, 71  
  - **node distances:**  
    - **node 0:** 0, 1, 2, 3  
    - **node 1:** 0, 10, 11, 21, 21  
    - **node 2:** 0, 10, 11, 21, 21  
    - **node 3:** 0, 10, 11, 21, 21  

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5220S, 2.70GHz)

SPECrate®2017_int_base = 204
SPECrate®2017_int_peak = 212

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

1:  11  10  21  21
2:  21  21  10  11
3:  21  21  11  10

From /proc/meminfo
MemTotal: 790930536 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 5 Sep 14 04:31

SPEC is set to: /home/cpu2017
  Filesystem  Type  Size  Used Avail Use% Mounted on
  /dev/sda3    xfs  324G  55G  270G  17%  /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. C240M5.4.0.4c.0.0411190411 04/11/2019
  Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5220S, 2.70GHz)

COMPILER VERSION NOTES

C
502.gcc_r(peak)

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C
500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
525.x264_r(base, peak) 557.xz_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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502.gcc_r(peak)

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C
500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++
523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++
520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5220S, 2.70GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5220S, 2.70GHz)

SPECrater®2017_int_base = 204
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
<p>| C++ | 523.xalancbmk_r(peak) |
| Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416 |</p>
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<tr>
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<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

(Continued on next page)
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**Base Portability Flags (Continued)**

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<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

**Base Optimization Flags**

**C benchmarks:**

- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

**C++ benchmarks:**

- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

**Fortran benchmarks:**

- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

**Peak Compiler Invocation**

**C benchmarks (except as noted below):**

icc -m64 -std=c11


**C++ benchmarks (except as noted below):**

icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5220S, 2.70GHz)

SPECrate®2017_int_base = 204
SPECrate®2017_int_peak = 212

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

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Peak Optimization Flags (Continued)

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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