Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230N, 2.30GHz)

SPECrate®2017_fp_base = 218
SPECrate®2017_fp_peak = 222

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019
Test Date: Sep-2019

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<td>554.roms_r</td>
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---

Hardware
CPU Name: Intel Xeon Gold 6230N
Max MHz: 3500
Nominal: 2300
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 27.5 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.3 released Mar-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: --
## Results Table

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</table>

### Submit Notes

The `numactl` mechanism was used to bind copies to processors. The `config` file option 'submit' was used to generate `numactl` commands to bind each copy to a specific processor.

For details, please see the `config` file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by `runcpu` before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
```

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

```
Files system page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through `numactl` i.e.:

```
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230N, 2.30GHz)

SPECCrate®2017_fp_base = 218
SPECCrate®2017_fp_peak = 222

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-2vgg Sat Sep 14 06:15:31 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6230N CPU @ 2.30GHz
  2  "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
```

From lscpu:
```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6230N CPU @ 2.30GHz
Stepping: 7
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230N, 2.30GHz)

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SPECrate®2017_fp_base = 218
SPECrate®2017_fp_peak = 222

Platform Notes (Continued)

CPU MHz: 2300.000
CPU max MHz: 3500.000
CPU min MHz: 1000.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-2, 5, 6, 10-12, 15, 16, 40-42, 45, 46, 50-52, 55, 56
NUMA node1 CPU(s): 3, 4, 7-9, 13, 14, 17-19, 43, 44, 47-49, 53, 54, 57-59
NUMA node2 CPU(s): 20-22, 25, 26, 30-32, 35, 36, 60-62, 65, 66, 70-72, 75, 76
NUMA node3 CPU(s): 23, 24, 27-29, 33, 34, 37-39, 63, 64, 67-69, 73, 74, 77-79
Flags: fpu vme de pse mce cmov pat pse36 clflush dts acpica mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmpref perf_refnfreq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebpxcat_l3 cd_l3 invpcid_single mba tpr_shadow vnni flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx mpx rdt_a avx512f avx512dq rdseed adx smap cldflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsave os vptpa xgetbv xsavec xsaveopt cqm_llc cmq_opcucll cqm_mbm_total cqm_mbm_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pkg ospke avx512_vnni arch_capabilities ssbd

/cache/cpuinfo cache data
cache size : 28160 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
node 0 size: 192102 MB
node 0 free: 180149 MB
node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
node 1 size: 193526 MB
node 1 free: 185002 MB
node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
node 2 size: 193526 MB
node 2 free: 184954 MB
node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
node 3 size: 193496 MB
node 3 free: 185042 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230N, 2.30GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrater®2017_fp_base = 218
SPECrater®2017_fp_peak = 222

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

1:  11  10  21  21
2:  21  21  10  11
3:  21  21  11  10

From /proc/meminfo
MemTotal: 791196780 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-2vgg 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 13 21:32
SPEC is set to: /home/cpu2017

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.3.34.0301190218 03/01/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
## Cisco Systems

**Cisco UCS C240 M5 (Intel Xeon Gold 6230N, 2.30GHz)**

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**CPU2017 License:** 9019  
**CPU2017 License:**  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Apr-2019  
**Tested by:** Cisco Systems  
**Software Availability:** May-2019

### Compiler Version Notes

<table>
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<th>Compiler</th>
<th>Programs (base, peak)</th>
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<tr>
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<td>C++, C</td>
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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230N, 2.30GHz)

SPEC CPU®2017 Floating Point Rate Result

Compiler Version Notes (Continued)

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64

(Continued on next page)
# SPEC CPU®2017 Floating Point Rate Result

## Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230N, 2.30GHz)

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### Base Portability Flags (Continued)

- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

**C++ benchmarks:**
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

**Fortran benchmarks:**
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

**Benchmarks using both Fortran and C:**
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

**Benchmarks using both C and C++:**
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

**Benchmarks using Fortran, C, and C++:**
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

### Peak Compiler Invocation

**C benchmarks:**
- icc -m64 -std=c11

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230N, 2.30GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

538.imagick_r: -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230N, 2.30GHz)  

SPECrater®2017_fp_base = 218
SPECrater®2017_fp_peak = 222

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Test Date: Sep-2019  
Tested by: Cisco Systems  
Hardware Availability: Apr-2019  
Software Availability: May-2019

Peak Optimization Flags (Continued)

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230N, 2.30GHz)

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