### Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

**CPU 2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jul-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

<table>
<thead>
<tr>
<th>Program</th>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>112</td>
<td>244</td>
<td>Not Run</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>112</td>
<td>239</td>
<td></td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>112</td>
<td>380</td>
<td></td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>112</td>
<td>192</td>
<td></td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>112</td>
<td>310</td>
<td></td>
</tr>
<tr>
<td>525.x264_r</td>
<td>112</td>
<td>632</td>
<td></td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>112</td>
<td>256</td>
<td></td>
</tr>
<tr>
<td>541.leela_r</td>
<td>112</td>
<td>247</td>
<td></td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>112</td>
<td>631</td>
<td></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>112</td>
<td>205</td>
<td></td>
</tr>
</tbody>
</table>

---

### Hardware

- **CPU Name:** Intel Xeon Platinum 8276L  
- **Max MHz:** 4000  
- **Nominal:** 2200  
- **Enabled:** 56 cores, 2 chips, 2 threads/core  
- **Orderable:** 1.2 chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 38.5 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
- **Storage:** 1 x 240G SSD SATA  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
  4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.0.4b released Apr-2019  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** None  
- **Power Management:** --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

**SPEC CPU®2017 Integer Rate Result**

Copyright 2017-2020 Standard Performance Evaluation Corporation

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jul-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>112</td>
<td>762</td>
<td>234</td>
<td>761</td>
<td>234</td>
<td>762</td>
<td>234</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>112</td>
<td>660</td>
<td>240</td>
<td>669</td>
<td>237</td>
<td>663</td>
<td>239</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>112</td>
<td>476</td>
<td>380</td>
<td>477</td>
<td>380</td>
<td>476</td>
<td>380</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>112</td>
<td>766</td>
<td>192</td>
<td>766</td>
<td>192</td>
<td>766</td>
<td>192</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>112</td>
<td>378</td>
<td>313</td>
<td>382</td>
<td>310</td>
<td>382</td>
<td>310</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>112</td>
<td>312</td>
<td>629</td>
<td>310</td>
<td>632</td>
<td>309</td>
<td>635</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>112</td>
<td>502</td>
<td>256</td>
<td>502</td>
<td>256</td>
<td>501</td>
<td>256</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>112</td>
<td>751</td>
<td>247</td>
<td>752</td>
<td>247</td>
<td>755</td>
<td>246</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>112</td>
<td>465</td>
<td>631</td>
<td>466</td>
<td>630</td>
<td>465</td>
<td>631</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>112</td>
<td>590</td>
<td>205</td>
<td>590</td>
<td>205</td>
<td>590</td>
<td>205</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 303**  
**SPECrate®2017_int_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3>/proc/sys/vm/drop_caches  
runcpu command invoked through numactl i.e.:  
umactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECraten int_base = 303
SPECraten int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618b0910f
running on linux-bo6o Thu Sep 5 10:34:57 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8276L CPU @ 2.20GHz
  2 "physical id"s (chips)
  112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 112
On-line CPU(s) list: 0-111
Thread(s) per core: 2
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8276L CPU @ 2.20GHz
Stepping: 7

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jul-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPECrate®2017_int_base = 303
SPECrate®2017_int_peak = Not Run

Platform Notes (Continued)

CPU MHz: 2200.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 39424K
NUMA node0 CPU(s): 0-3, 7-9, 14-17, 21-23, 56-59, 63-65, 70-73, 77-79
NUMA node1 CPU(s): 4-6, 10-13, 18-20, 24-27, 60-62, 66-69, 74-76, 80-83
NUMA node2 CPU(s): 28-31, 35-37, 42-45, 49-51, 84-87, 91-93, 98-101, 105-107
NUMA node3 CPU(s): 32-34, 38-41, 46-48, 52-55, 88-90, 94-97, 102-104, 108-111
Flags: fpu vme de pse mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pppin mba tpr_shadow vmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ireds invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 7 8 9 14 15 16 17 21 22 23 56 57 58 59 63 64 65 70 71 72 73 77 78 79
node 0 size: 191929 MB
node 0 free: 191530 MB
node 1 cpus: 4 5 6 10 11 12 13 18 19 20 24 25 26 27 60 61 62 66 67 68 69 74 75 76 80 81 82 83
node 1 size: 193491 MB
node 1 free: 193245 MB
node 2 cpus: 28 29 30 31 35 36 37 42 43 44 45 49 50 51 84 85 86 87 91 92 93 98 99 100 101 105 106 107
node 2 size: 193520 MB
node 2 free: 193278 MB
node 3 cpus: 32 33 34 38 39 40 41 46 47 48 52 53 54 55 88 89 90 94 95 96 97 102 103 104 108 109 110 111
node 3 size: 193517 MB

(Continued on next page)
**Platform Notes (Continued)**

- **node 3 free:** 193279 MB
- **node distances:**
  - node: 0 1 2 3
  - 0: 10 11 21 21
  - 1: 11 10 21 21
  - 2: 21 21 10 11
  - 3: 21 21 11 10

From `/proc/meminfo`
- **MemTotal:** 790998420 kB
- **HugePages_Total:** 0
- **Hugepagesize:** 2048 kB

From `/etc/*release*` /`/etc/*version*`
- **os-release:**
  - NAME="SLES"
  - VERSION="15"
  - VERSION_ID="15"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15"
  - ID="sles"
  - ID_LIKE="suse"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:15"

**uname -a:**
- Linux linux-bo6o 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
- x86_64 x86_64 x86_64 GNU/Linux

**run-level 3 Sep 5 10:14**

**SPEC is set to:** `/home/cpu2017`
- **Filesystem** Type Size Used Avail Use% Mounted on
  - `/dev/sdcl` btrfs 224G 15G 208G 7% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

**BIOS** Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019

**Memory:**
- 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECratenetbase = 303
SPECratenetpeak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes

C
500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
525.x264_r(base) 557.xz_r(base)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++
520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
541.leela_r(base)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran
548.exchange2_r(base)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECrate®2017_int_base = 303
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Portability Flags (Continued)

523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leea_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-09-05 13:34:56:0400.
Report generated on 2020-12-15 17:56:54 by CPU2017 PDF formatter v6255.
Originally published on 2019-10-01.