### SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**  
Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)  

<table>
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<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Jul-2019</th>
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<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
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<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
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**SPECrate®2017_fp_base = 259**  
**SPECrate®2017_fp_peak = Not Run**

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base (259)</th>
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<tbody>
<tr>
<td>503.bwaves_r</td>
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<tr>
<td>507.cactuBSSN_r</td>
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<td>508.namd_r</td>
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<td>510.parest_r</td>
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<td>527.cam4_r</td>
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<td>538.imagick_r</td>
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<td>544.nab_r</td>
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<tr>
<td>549.fotonik3d_r</td>
</tr>
<tr>
<td>554.roms_r</td>
</tr>
</tbody>
</table>

### Hardware

**CPU Name:** Intel Xeon Platinum 8276L  
**Max MHz:** 4000  
**Nominal:** 2200  
**Enabled:** 56 cores, 2 chips, 2 threads/core  
**Orderable:** 1,2 chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 1 MB I+D on chip per core  
**L3:** 38.5 MB I+D on chip per chip  
**Other:** None  
**Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
**Storage:** 1 x 1.9 TB SSD SAS  
**Other:** None

### Software

**OS:** SUSE Linux Enterprise Server 15 (x86_64)  
**Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
**Parallel:** No  
**Firmware:** Version 4.0.4b released Apr-2019  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** Not Applicable  
**Other:** None  
**Power Management:** --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

| SPECrate®2017_fp_base = 259 |
| SPECrate®2017_fp_peak = Not Run |

General Notes (Continued)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-bo6o Thu Sep  5 15:39:37 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8276L CPU @ 2.20GHz
  2  "physical id"s (chips)
  112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 112
On-line CPU(s) list: 0-111
Thread(s) per core: 2
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel

(Continued on next page)
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**SPECrates**  
- **SPECrate®2017_fp_base =** 259  
- **SPECrate®2017_fp_peak =** Not Run

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**Platform Notes (Continued)**

- CPU family: 6  
- Model: 85  
- Model name: Intel(R) Xeon(R) Platinum 8276L CPU @ 2.20GHz  
- Stepping: 7  
- CPU MHz: 2200.000  
- CPU max MHz: 4000.0000  
- CPU min MHz: 1000.0000  
- BogoMIPS: 4400.00  
- Virtualization: VT-x  
- L1d cache: 32K  
- L1i cache: 32K  
- L2 cache: 1024K  
- L3 cache: 39424K  
- NUMA node0 CPU(s): 0-3,7-9,14-17,21-23,56-59,70-73,77-79  
- NUMA node1 CPU(s): 4-6,10-13,18-20,24-27,60-62,66-69,74-76,80-83  
- NUMA node2 CPU(s): 28-31,35-37,42-45,49-51,84-87,91-93,98-101,105-107  
- NUMA node3 CPU(s): 32-34,38-41,46-48,52-55,88-90,94-97,102-104,108-111  
- Flags: fpu vme de pse mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperf perfctr tscknown_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault ebp cat_i3 cdp_l3 invpcid_single intel_ppi mba tpr_shadow vni flexpriority ept vpid fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 edsms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsavesopt xsaveopt xaxcgetbv1 xsaves cqm_llc cqm_occucp_l1c cqm_mbm_total cqm_mbm_local ibpb ibrs ibrs tdp dmtr ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

**/proc/cpuinfo cache data**  
- cache size: 39424 KB

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(Continued on next page)
Platform Notes (Continued)

node 2 free: 193002 MB
node 3 cpus: 32 33 34 38 39 40 41 46 47 48 52 53 54 55 88 89 90 94 95 96 97 102 103 104 108 109 110 111
node 3 size: 193517 MB
node 3 free: 193055 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 790998420 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-bo6o 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Sep 5 10:14

SPEC is set to: /home/cpu2017
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sdc1 btrfs 224G 15G 208G 7% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

  BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
  Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
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Compiler Version Notes

<table>
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<th>Language</th>
<th>Compiler Version</th>
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<tbody>
<tr>
<td>C</td>
<td>519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)</td>
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<tr>
<td></td>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
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<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
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| C++      | 508.namd_r(base) 510.parest_r(base) |
|          | Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 |
|          | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |

| C++, C   | 511.povray_r(base) 526.blender_r(base) |
|          | Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 |
|          | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |

| C++, C, Fortran | 507.cactuBSSN_r(base) |
|                | Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 |
|                | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |

| Fortran    | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base) |
|           | Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 |
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Compiler Version Notes (Continued)
==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char

(Continued on next page)
Base Portability Flags (Continued)

527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-09-05 18:39:36-0400.


Originally published on 2019-10-01.