Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5215M, 2.50GHz)

SPECspeed®2017_fp_base = 90.0
SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Threads

| 603.bwaves_s | 20 | 97.5 |
| 607.cactuBSSN_s | 20 | 75.0 |
| 619.lbm_s | 20 | 85.0 |
| 621.wrf_s | 20 | 52.4 |
| 627.cam4_s | 20 | 62.1 |
| 628.pop2_s | 20 | 65.7 |
| 638.imagick_s | 20 | 122 |
| 644.nab_s | 20 | 70.0 |
| 649.fotonik3d_s | 20 | 82.2 |

Hardware
CPU Name: Intel Xeon Gold 5215M
Max MHz: 3400
Nominal: 2500
Enabled: 20 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I+ 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 13.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
Storage: 1 x 960 GB SATA M.2 SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4b released Apr-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: --
## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems

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**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Base Seconds</th>
<th>Base Ratio</th>
<th>Peak Seconds</th>
<th>Peak Ratio</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>20</td>
<td>159</td>
<td>370</td>
<td>159</td>
<td>370</td>
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<tr>
<td>607.cactuBSSN_s</td>
<td>20</td>
<td>171</td>
<td>97.5</td>
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<td>97.5</td>
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<tr>
<td>619.lbm_s</td>
<td>20</td>
<td>69.7</td>
<td>75.2</td>
<td>70.0</td>
<td>74.9</td>
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<tr>
<td>621.wrf_s</td>
<td>20</td>
<td>157</td>
<td>84.2</td>
<td>155</td>
<td>85.3</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>20</td>
<td>169</td>
<td>52.4</td>
<td>169</td>
<td>52.5</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>20</td>
<td>193</td>
<td>61.6</td>
<td>191</td>
<td>62.2</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>20</td>
<td>219</td>
<td>65.8</td>
<td>219</td>
<td>65.7</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>20</td>
<td>143</td>
<td>122</td>
<td>143</td>
<td>122</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>20</td>
<td>130</td>
<td>70.0</td>
<td>130</td>
<td>70.1</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>20</td>
<td>191</td>
<td>82.3</td>
<td>192</td>
<td>81.9</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_fp_base =** 90.0  
**SPECspeed®2017_fp_peak =** Not Run

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
Memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:
  
sync; echo 3> /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

Intel HyperThreading Technology set to Disabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5215M, 2.50GHz)

SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-3xnd Fri Sep  6 15:49:15 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5215M CPU @ 2.50GHz
2 "physical id"s (chips)
20 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings  : 10
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 20
On-line CPU(s) list: 0-19
Thread(s) per core: 1
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5215M CPU @ 2.50GHz
Stepping: 6
CPU MHz: 2500.000
CPU max MHz: 3400.0000
CPU min MHz: 1000.0000
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9
(Continued on next page)
Cisco Systems  
Cisco UCS B200 M5 (Intel Xeon Gold 5215M, 2.50GHz)  

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Test Date: Aug-2019  
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Software Availability: May-2019

Platform Notes (Continued)

NUMA node1 CPU(s): 10-19  
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ews invpcid rtm cqm mpx rt_d a
avx512f rdseed adx smap clflushopt clwb intel_pt avx512sd avx512bw avx512vl
xsaves opt xsave xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local ibpbb ibrs stibp dtherm ida pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9
  node 0 size: 385589 MB
  node 0 free: 380097 MB
  node 1 cpus: 10 11 12 13 14 15 16 17 18 19
  node 1 size: 387046 MB
  node 1 free: 382942 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 791179536 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

(Continued on next page)
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Tested by: Cisco Systems

Platform Notes (Continued)

uname -a:
 Linux linux-3xnd 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Sep 6 08:35

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb4 xfs 100G 19G 81G 19% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

<table>
<thead>
<tr>
<th>Compiler Version</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
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<td>C</td>
<td>619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)</td>
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<td>Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td>Copyright (C)</td>
<td>1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>C++, C, Fortran</td>
<td>607.cactuBSSN_s(base)</td>
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<tr>
<td>Intel(R) C++</td>
<td>Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
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<tr>
<td>Intel(R) Fortran</td>
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<td>Fortran</td>
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(Continued on next page)
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Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran, C
| 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactusBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
   -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64

(Continued on next page)
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Base Portability Flags (Continued)
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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