Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 5218N, 2.30GHz)

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Aug-2019</th>
</tr>
</thead>
<tbody>
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<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
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<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base = 176</th>
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<tbody>
<tr>
<td>500.perlbench_r 64</td>
<td></td>
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<tr>
<td>502.gcc_r 64</td>
<td>146</td>
</tr>
<tr>
<td>505.mcf_r 64</td>
<td>232</td>
</tr>
<tr>
<td>520.omnetpp_r 64</td>
<td>119</td>
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<tr>
<td>523.xalancbmk_r 64</td>
<td>198</td>
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<tr>
<td>525.x264_r 64</td>
<td>336</td>
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<tr>
<td>531.deepsjeng_r 64</td>
<td>143</td>
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<tr>
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<td></td>
</tr>
<tr>
<td>557.xz_r 64</td>
<td>118</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Gold 5218N</td>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
</tr>
<tr>
<td>Max MHz: 3700</td>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Nominal: 2300</td>
<td>Parallel: No</td>
</tr>
<tr>
<td>Enabled: 32 cores, 2 chips, 2 threads/core</td>
<td>Firmware: Version 4.0.4b released Apr-2019</td>
</tr>
<tr>
<td>Orderable: 1,2 Chips</td>
<td>File System: xfs</td>
</tr>
<tr>
<td>Cache L1: 32 KB I+32 KB D on chip per core</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>L2: 1 MB I+D on chip per core</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>L3: 22 MB I+D on chip per chip</td>
<td>Peak Pointers: Not Applicable</td>
</tr>
<tr>
<td>Other: None</td>
<td>Other: None</td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)</td>
<td>Power Management: --</td>
</tr>
<tr>
<td>Storage: 1 x 1.9 TB SSD SAS</td>
<td></td>
</tr>
</tbody>
</table>

SPEC CPU®2017 Integer Rate Result
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Cisco Systems

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Results Table

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<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>gcc_r</td>
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<td>232</td>
<td>447</td>
<td>232</td>
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<td>omnetpp_r</td>
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<td>xalancbmk_r</td>
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<tr>
<td>x264_r</td>
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<td>337</td>
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<td>336</td>
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<td>336</td>
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<tr>
<td>deepsjeng_r</td>
<td>64</td>
<td>512</td>
<td>143</td>
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<td>512</td>
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<td>leela_r</td>
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<td>762</td>
<td>139</td>
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<td>139</td>
<td>766</td>
<td>138</td>
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<tr>
<td>exchange2_r</td>
<td>64</td>
<td>479</td>
<td>350</td>
<td>478</td>
<td>351</td>
<td>479</td>
<td>350</td>
</tr>
<tr>
<td>xz_r</td>
<td>64</td>
<td>586</td>
<td>118</td>
<td>587</td>
<td>118</td>
<td>587</td>
<td>118</td>
</tr>
</tbody>
</table>

| SPECrate®2017_int_base = 176 |
| SPECrate®2017_int_peak = Not Run |

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 5218N, 2.30GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

is mitigated in the system as tested and documented.

Platform Notes

Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-3xnd Wed Sep 11 08:05:27 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5218N CPU @ 2.30GHz
  2 "physical id"s (chips)
  64 "processors"
core(s), siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218N CPU @ 2.30GHz
Stepping: 6
CPU MHz: 2300.000
CPU max MHz: 3900.000

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

### Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 5218N, 2.30GHz)

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### SPECrate®2017_int_base = 176

### SPECrate®2017_int_peak = Not Run

#### Platform Notes (Continued)

- CPU min MHz: 1000.0000
- BogoMIPS: 4600.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 22528K
- NUMA node0 CPU(s): 0-3, 8-11, 32-35, 40-43
- NUMA node1 CPU(s): 4-7, 12-15, 36-39, 44-47
- NUMA node2 CPU(s): 16-19, 24-27, 48-51, 56-59
- NUMA node3 CPU(s): 20-23, 28-31, 52-55, 60-63
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
- pat pse3 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
- lm constant_tsc arch_perfmon pebs bts rep_good xtopology nonstop_tsc cpuid
- aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 sse3
- sdbg fma cx16 xtpr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt
- tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
- epb cat_l3 cdp_l3 invpcid_single intel_pni mba tpr_shadow vmx
- fenv1 flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
- cpqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
- avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cpqm_llc cpqm_occ Hipp cpqm_mbb_local
- lbpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
- ospke avx512_vnni arch_capabilities ssbd

```
/proc/cpuinfo cache data
cache size : 22528 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 8 9 10 11 32 33 34 35 40 41 42 43
  node 0 size: 192091 MB
  node 0 free: 191539 MB
  node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
  node 1 size: 193522 MB
  node 1 free: 193278 MB
  node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
  node 2 size: 193493 MB
  node 2 free: 193279 MB
  node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
  node 3 size: 193519 MB
  node 3 free: 193273 MB
  node distances:
    node   0   1   2   3
    0: 10 11 12 21
    1: 11 10 21 21
    2: 21 21 10 11
```

(Continued on next page)
Cisco Systems

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Platform Notes (Continued)

3: 21 21 11 10

From /proc/meminfo
MemTotal: 791170736 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME=cpe:/o:suse:sles:15

uname -a:
Linux linux-3xnd 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Sep 11 07:32

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb4 xfs 100G 13G 88G 13% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C     500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
     525.x264_r(base) 557.xz_r(base)
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416

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# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

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**Cisco Systems**

**SPEC CPU®2017 Integer Rate Result**

**Cisco UCS B200 M5 (Intel Xeon Gold 5218N, 2.30GHz)**

**SPECrate®2017_int_base = 176**

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**CPU2017 License:** 9019  
**Test Date:** Aug-2019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

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**Compiler Version Notes (Continued)**

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**C++**

<table>
<thead>
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<tr>
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</tr>
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</tr>
<tr>
<td>541.leela_r(base)</td>
</tr>
</tbody>
</table>

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Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
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**Fortran**

<table>
<thead>
<tr>
<th>Benchmark</th>
</tr>
</thead>
<tbody>
<tr>
<td>548.exchange2_r(base)</td>
</tr>
</tbody>
</table>

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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
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---

## Base Compiler Invocation

**C benchmarks:**

`icc -m64 -std=c11`

**C++ benchmarks:**

`icpc -m64`

**Fortran benchmarks:**

`ifort -m64`

---

## Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64
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Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-09-11 11:05:26-0400.
Report generated on 2020-07-02 20:41:10 by CPU2017 PDF formatter v6255.
Originally published on 2019-10-01.