## SPEC CPU®2017 Integer Rate Result

### Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

| Copies | 0 | 20 | 40 | 60 | 80 | 100 | 120 | 140 | 160 | 180 | 200 | 220 | 240 | 260 | 280 | 300 | 320 | 340 | 360 | 380 | 400 | 420 | 440 | 460 | 480 | 500 | 520 | 540 | 560 | 580 | 600 | 620 | 640 | 660 | 680 |
|--------|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 500.perlbench_r | 72 | ![171] | ![181] |
| 502.gcc_r | 72 | ![296] |
| 505.mcf_r | 72 | ![470] |
| 520.omnetpp_r | 72 | ![145] |
| 523.xalancbmk_r | 72 |
| 525.x264_r | 72 | ![455] |
| 531.deepsjeng_r | 72 | ![147] |
| 541.leela_r | 72 | ![180] |
| 548.exchange2_r | 72 | ![464] |
| 557.xz_r | 72 | ![489] |

### Hardware

- **CPU Name:** Intel Xeon Gold 6240Y
- **Max MHz:** 3900
- **Nominal:** 2600
- **Enabled:** 36 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 24.75 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
  4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --

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**SPECrater®2017_int_base = 226**

**SPECrater®2017_int_peak = Not Run**
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

SPECrate®2017_int_base = 226
SPECrate®2017_int_peak = Not Run

Results Table

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</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
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Cisco UCS B200 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
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<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

| CPU2017 License: | 9019 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |

#### General Notes (Continued)

is mitigated in the system as tested and documented.

#### Platform Notes

BIOS Settings:
- Intel HyperThreading Technology set to Enabled
- SNC set to Enabled

Power Performance Tuning set to OS Controls
- Patrol Scrub set to Disabled
- Sysinfo program /home/cpu2017/bin/sysinfo
- Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
- running on linux-5vrl Wed Sep 11 08:06:50 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```plaintext
model name : Intel(R) Xeon(R) Gold 6240C CPU @ 2.60GHz
  2 "physical id"s (chips)
  72 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 18
  siblings : 36
  physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
```

From lscpu:

```plaintext
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 2
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240C CPU @ 2.60GHz
Stepping: 6
CPU MHz: 2600.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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SPECrate\textsuperscript{\textregistered}2017\_int\_base = 226
SPECrate\textsuperscript{\textregistered}2017\_int\_peak = Not Run

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-2,5,6,9,10,14,15,36-38,41,42,45,46,50,51
NUMA node1 CPU(s): 3,4,7,8,11-13,16,17,39,40,43,44,47-49,52,53
NUMA node2 CPU(s): 18-20,23,24,27,28,32,33,54-56,59,60,63,64,68,69
NUMA node3 CPU(s): 21,22,25,26,29-31,34,35,57,58,61,62,65-67,70,71
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 sse3 sdbg fma cx16 xtpr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_i3 cdpr_l3 invpcid_single intel.ppin tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavec qmmf llc qmmf_occq llc qmmf_mbm_total qmmf_mbm_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

node 0 cpus: 0 1 2 3
node 0 size: 192901 MB
node 0 free: 191758 MB
node 1 cpus: 4 7 8 11 12 13 16 17 39 40 43 44 47 49 52 53
node 1 size: 193522 MB
node 1 free: 193289 MB
node 2 cpus: 18 19 20 23 24 27 28 32 33 54 55 56 59 60 63 64 68 69
node 2 size: 193493 MB
node 2 free: 193258 MB
node 3 cpus: 21 22 25 26 29 30 31 34 35 57 58 61 62 65 66 67 70 71
node 3 size: 193519 MB
node 3 free: 193272 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

<table>
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<th>CPU2017 License:</th>
<th>9019</th>
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<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
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<td>Tested by:</td>
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<tr>
<td>Test Date:</td>
<td>Aug-2019</td>
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<td>May-2019</td>
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</tbody>
</table>

SPECraten®2017_int_base = 226
SPECraten®2017_int_peak = Not Run

Platform Notes (Continued)

From /proc/meminfo
MemTotal:       791169204 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-5vrl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Sep 11 07:35

SPEC is set to: /home/cpu2017
  Filesystem     Type   Size  Used Avail Use% Mounted on
  /dev/sdb1      btrfs  224G   15G  208G   7% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
  Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
The marketing name for the processor in this result, which appears in the CPU name and hardware
model areas, is different from sysinfo because a pre-production processor was used. The
pre-production processor differs from the production processor in name only.

Compiler Version Notes

==============================================================================
| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)  
<table>
<thead>
<tr>
<th></th>
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<td>525.x264_r(base) 557.xz_r(base)</td>
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(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

SPEC CPU®2017 Integer Rate Result
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SPECrated®2017_int_base = 226
SPECrated®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

--------------------------------------------------------------------------------

C++ | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
    | 541.leela_r(base)
--------------------------------------------------------------------------------

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

--------------------------------------------------------------------------------

Fortran | 548.exchange2_r(base)
--------------------------------------------------------------------------------

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

--------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64

(Continued on next page)
Spec CPU®2017 Integer Rate Result

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Cisco UCS B200 M5 (Intel Xeon Gold 6240Y, 2.60GHz) SPECrate®2017_int_base = 226
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9019
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Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Portability Flags (Continued)
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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Tested with SPEC CPU®2017 v1.0.2 on 2019-09-11 11:06:49-0400.
Originally published on 2019-10-07.