Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5218N, 2.30GHz)

SPECspeed®2017_int_base = 9.87
SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Threads

| 600.perlbench_s | 32 | 8.84 | 9.71 |
| 602.gcc_s       | 32 |       | 12.6 |
| 605.mcf_s       | 32 |       | 7.41 |
| 620.omnetpp_s   | 32 |       |       |
| 623.xalancbmk_s | 32 |       | 12.4 |
| 625.x264_s     | 32 |       | 11.6 |
| 631.deepsjeng_s| 32 |       | 5.57 |
| 641.leea_s     | 32 |       | 4.78 |
| 648.exchange2_s| 32 |       | 16.7 |
| 657.xz_s       | 32 |       | 22.3 |

Hardware
CPU Name: Intel Xeon Gold 5218N
Max MHz: 3700
Nominal: 2300
Enabled: 32 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 22 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
          Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4b released Apr-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: --
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Base</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>32</td>
<td>262</td>
<td>6.78</td>
<td>260</td>
<td>6.84</td>
<td>258</td>
<td>6.89</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>32</td>
<td>410</td>
<td>9.71</td>
<td>411</td>
<td>9.68</td>
<td>410</td>
<td>9.71</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>32</td>
<td>376</td>
<td>12.5</td>
<td>374</td>
<td>12.6</td>
<td>374</td>
<td>12.6</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>32</td>
<td>220</td>
<td>7.41</td>
<td>222</td>
<td>7.36</td>
<td>220</td>
<td>7.41</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>32</td>
<td>115</td>
<td>12.4</td>
<td>114</td>
<td>12.4</td>
<td>114</td>
<td>12.4</td>
<td></td>
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</tr>
<tr>
<td>625.x264_s</td>
<td>32</td>
<td>152</td>
<td>11.6</td>
<td>152</td>
<td>11.6</td>
<td>152</td>
<td>11.6</td>
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</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>32</td>
<td>262</td>
<td>5.47</td>
<td>262</td>
<td>5.47</td>
<td>262</td>
<td>5.47</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>641.leela_s</td>
<td>32</td>
<td>357</td>
<td>4.78</td>
<td>357</td>
<td>4.78</td>
<td>357</td>
<td>4.78</td>
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<td>16.7</td>
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<tr>
<td>657.xz_s</td>
<td>32</td>
<td>277</td>
<td>22.3</td>
<td>277</td>
<td>22.3</td>
<td>277</td>
<td>22.3</td>
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</tbody>
</table>

Results appear in the order in which they were run.Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
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SPECspeed®2017_int_base = 9.87
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Platform Notes

Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-3xnd Sat Sep 14 09:34:52 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5218N CPU @ 2.30GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218N CPU @ 2.30GHz
Stepping: 6
CPU MHz: 2300.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

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Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
Flags: fpu vme de pse tsc mr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush ds acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdkg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdpl_13 invpcid_single intel_pmm mba tpr_shadow vmni flexpriority ept
vpid fsgsb the tsc_adjust bmon hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdts
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves xsavec xgetbv1 xsaves cqm_llc cqm_occup_11c cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida ar pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 385617 MB
node 0 free: 384869 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 387016 MB
node 1 free: 382631 MB
node distances:
node 0 1
 0: 10 21
 1: 21 10

From /proc/meminfo
MemTotal: 791177224 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"

(Continued on next page)
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Platform Notes (Continued)

ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-3xnd 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Sep 14 07:13
SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb4 xfs 100G 16G 85G 16% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
| 625.x264_s(base) 657.xz_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

C++     | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
| 641.leela_s(base)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

Fortran | 648.exchange2_s(base)
(Continued on next page)
Cisco Systems
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SPEC®2017 CPU Integer Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

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Compiler Version Notes (Continued)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
  icc -m64 -std=c11

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64

Base Portability Flags

Base Optimization Flags

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### Base Optimization Flags (Continued)

Fortran benchmarks:
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links: