## SPEC CPU®2017 Integer Speed Result

### Hardware

- **CPU Name:** Intel Xeon Gold 6240Y
- **Max MHz:** 3900
- **Nominal:** 2600
- **Enabled:** 36 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I+D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 24.75 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 240G SSD SATA
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --

### Test Details

- **CPU2017 License:** 9019
- **Test Sponsor:** Cisco Systems
- **Tested by:** Cisco Systems
- **Test Date:** Aug-2019
- **Hardware Availability:** Apr-2019
- **Software Availability:** May-2019

### Performance Results

<table>
<thead>
<tr>
<th>SPEC Benchmark</th>
<th>Threads</th>
<th>Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>36</td>
<td>6.85</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>36</td>
<td>9.49</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>36</td>
<td>12.5</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>36</td>
<td>7.66</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>36</td>
<td>12.4</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>36</td>
<td>14.2</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>36</td>
<td>5.45</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>36</td>
<td>4.78</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>36</td>
<td>16.7</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>36</td>
<td>22.7</td>
</tr>
</tbody>
</table>

### SPECspeed®2017

- **SPECspeed®2017_int_base = 10.1**
- **SPECspeed®2017_int_peak = Not Run**
Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

SPECspeed®2017_int_base = 10.1
SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
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<th>Ratio</th>
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</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>36</td>
<td>259</td>
<td>6.84</td>
<td>259</td>
<td>6.85</td>
<td>258</td>
<td>6.87</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>36</td>
<td>410</td>
<td>9.71</td>
<td>413</td>
<td>9.65</td>
<td>411</td>
<td>9.69</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>36</td>
<td>375</td>
<td>12.6</td>
<td>376</td>
<td>12.5</td>
<td>377</td>
<td>12.5</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>36</td>
<td>213</td>
<td>7.66</td>
<td>214</td>
<td>7.61</td>
<td>209</td>
<td>7.79</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>36</td>
<td>114</td>
<td>12.4</td>
<td>114</td>
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<td>12.4</td>
</tr>
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<td>36</td>
<td>125</td>
<td>14.2</td>
<td>125</td>
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<td>36</td>
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<td>5.45</td>
<td>263</td>
<td>5.46</td>
<td>263</td>
<td>5.45</td>
</tr>
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<td>36</td>
<td>357</td>
<td>4.78</td>
<td>357</td>
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</tr>
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<td>178</td>
<td>16.5</td>
<td>176</td>
<td>16.7</td>
</tr>
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<td>36</td>
<td>272</td>
<td>22.8</td>
<td>272</td>
<td>22.7</td>
<td>272</td>
<td>22.7</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3>/proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**
Cisco UCS B200 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

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<th>SPECspeed®2017_int_peak</th>
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<tr>
<td>10.1</td>
<td>Not Run</td>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes

**BIOS Settings:**
- Intel HyperThreading Technology set to Disabled
- SNC set to Disabled
- Power Performance Tuning set to OS Controls
- Patrol Scrub set to Disabled

**Sysinfo program** /home/cpu2017/bin/sysinfo  
**Rev:** r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
**running on linux-5vrl Sat Sep 14 09:33:25 2019**

**SUT (System Under Test) info as seen by some common utilities.**
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo:
- **model name:** Intel(R) Xeon(R) Gold 6240C CPU @ 2.60GHz
- **cpu cores:** 18  
- **siblings:** 18  
- **physical 0:** cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27  
- **physical 1:** cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
- **Architecture:** x86_64  
- **CPU op-mode(s):** 32-bit, 64-bit  
- **Byte Order:** Little Endian  
- **CPU(s):** 36  
- **On-line CPU(s) list:** 0-35  
- **Thread(s) per core:** 1  
- **Core(s) per socket:** 18  
- **Socket(s):** 2  
- **NUMA node(s):** 2  
- **Vendor ID:** GenuineIntel  
- **CPU family:** 6  
- **Model:** 85  
- **Model name:** Intel(R) Xeon(R) Gold 6240C CPU @ 2.60GHz  
- **Stepping:** 6  
- **CPU MHz:** 2600.000  
- **CPU max MHz:** 3900.0000  
- **CPU min MHz:** 1000.0000  
- **BogoMIPS:** 5200.00  
- **Virtualization:** VT-x  
- **L1d cache:** 32K  
- **L1i cache:** 32K  
- **L2 cache:** 1024K

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

**SPEC CPU®2017 Integer Speed Result**

**Specspeed®2017_int_base = 10.1**

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### Platform Notes (Continued)

L3 cache: 25344K  
NUMA node0 CPU(s): 0-17  
NUMA node1 CPU(s): 18-35  
Flags: fpum vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts msr ept est Bulldozer TSX NaN fdiv fpred idiv

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.

0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
node 0 size: 385588 MB
nenode 0 free: 385007 MB
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
node 1 size: 387045 MB
node 1 free: 382703 MB
node distances:
node 0: 10 21
0: 10 21
1: 21 10

From /proc/meminfo

MemTotal: 791176456 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*

os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
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Platform Notes (Continued)

uname -a:
   Linux linux-5vrl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
   x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Sep 14 07:14

SPEC is set to: /home/cpu2017

Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sdb1      btrfs  224G   18G  205G   8% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
   Memory:
      24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

The marketing name for the processor in this result, which appears in the CPU name and hardware
model areas, is different from sysinfo because a pre-production processor was used. The
pre-production processor differs from the production processor in name only.

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
| 625.x264_s(base) 657.xz_s(base)
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++     | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
| 641.leela_s(base)
==============================================================================

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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Cisco Systems
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CPU2017 License: 9019  Test Date:  Aug-2019
Test Sponsor:  Cisco Systems  Hardware Availability: Apr-2019
Tested by:  Cisco Systems  Software Availability: May-2019

Compiler Version Notes (Continued)
Fortran | 648.exchange2_s (base)
-------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-------------------------------------------------------------

Base Compiler Invocation
C benchmarks:
icec -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4

(Continued on next page)
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**Base Optimization Flags (Continued)**

**C++ benchmarks (continued):**
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

**Fortran benchmarks:**
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


---


For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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