### SPEC CPU®2017 Integer Rate Result

**Cisco Systems**  
Cisco UCS B200 M5 (Intel Xeon Gold 6240M, 2.60GHz)

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<thead>
<tr>
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<td>9019</td>
<td>Aug-2019</td>
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**SPECrate®2017_int_base = 227**  
**SPECrate®2017_int_peak = Not Run**

#### Hardware

- **CPU Name:** Intel Xeon Gold 6240M  
- **Max MHz:** 3900  
- **Nominal:** 2600  
- **Enabled:** 36 cores, 2 chips, 2 threads/core  
- **Orderable:** 1.2 Chips  
- **Cache L1:** 32 KB I+ 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 24.75 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
- **Storage:** 1 x 1.9 TB SSD SAS  
- **Other:** None

#### Software

- **OS:** SUSE Linux Enterprise Server 15 4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.0.4b released Apr-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** None  
- **Power Management:** --
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Hardware Availability: Apr-2019
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Results Table

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<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>72</td>
<td>658</td>
<td>174</td>
<td>664</td>
<td>173</td>
<td>665</td>
<td>172</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>72</td>
<td>571</td>
<td>178</td>
<td>569</td>
<td>179</td>
<td>574</td>
<td>178</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>72</td>
<td>395</td>
<td>295</td>
<td>397</td>
<td>293</td>
<td>395</td>
<td>295</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>72</td>
<td>646</td>
<td>146</td>
<td>646</td>
<td>146</td>
<td>646</td>
<td>146</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>72</td>
<td>314</td>
<td>242</td>
<td>314</td>
<td>242</td>
<td>315</td>
<td>241</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>72</td>
<td>276</td>
<td>456</td>
<td>276</td>
<td>457</td>
<td>278</td>
<td>453</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>72</td>
<td>435</td>
<td>190</td>
<td>433</td>
<td>191</td>
<td>433</td>
<td>191</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>72</td>
<td>646</td>
<td>184</td>
<td>655</td>
<td>182</td>
<td>647</td>
<td>184</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>72</td>
<td>402</td>
<td>470</td>
<td>400</td>
<td>471</td>
<td>401</td>
<td>470</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>72</td>
<td>518</td>
<td>150</td>
<td>518</td>
<td>150</td>
<td>517</td>
<td>151</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64;/home/cpu2017/lib/ia32;/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240M, 2.60GHz)

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

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### General Notes (Continued)

is mitigated in the system as tested and documented.

### Platform Notes

BIOS Settings:  
Intel HyperThreading Technology set to Enabled  
SNC set to Enabled  
Power Performance Tuning set to OS Controls  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9  
running on linux-db10 Wed Sep 4 15:10:41 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

- model name: Intel(R) Xeon(R) Gold 6240M CPU @ 2.60GHz  
- 2 "physical id"s (chips)  
- 72 "processors"  
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
  - cpu cores: 18  
  - siblings: 36  
  - physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27  
  - physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:

- Architecture: x86_64  
- CPU op-mode(s): 32-bit, 64-bit  
- Byte Order: Little Endian  
- CPU(s): 72  
- On-line CPU(s) list: 0-71  
- Thread(s) per core: 2  
- Core(s) per socket: 18  
- Socket(s): 2  
- NUMA node(s): 4  
- Vendor ID: GenuineIntel  
- CPU family: 6  
- Model: 85  
- Model name: Intel(R) Xeon(R) Gold 6240M CPU @ 2.60GHz  
- Stepping: 7  
- CPU MHz: 2600.000  
- CPU max MHz: 3900.0000  
- CPU min MHz: 1000.0000

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Platform Notes (Continued)

BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-2,5,6,9,10,14,15,36-38,41,42,45,46,50,51
NUMA node1 CPU(s): 3,4,7,8,11-13,16,17,39,40,43,44,47-49,52,53
NUMA node2 CPU(s): 18-20,23,24,27,28,32,33,34-36,59,60,63,64,68,69
NUMA node3 CPU(s): 21,22,25,26,29-31,34,35,57,58,61,62,65-67,70,71
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 cclfush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xptr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebpx cat_13 cdpl_13 invpcid_single intel_pipin tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavec qcm llc qcm_occup_llc qcm_mbm_total qcm_mbm_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

Available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 6 9 10 14 15 36 37 38 41 42 45 46 50 51
node 0 size: 191931 MB
node 0 free: 191608 MB
node 1 cpus: 3 4 7 8 11 12 13 16 17 39 40 43 44 47 48 49 52 53
node 1 size: 193522 MB
node 1 free: 193243 MB
node 2 cpus: 18 19 20 23 24 27 28 32 33 54 55 56 59 60 63 64 68 69
node 2 size: 193522 MB
node 2 free: 193280 MB
node 3 cpus: 21 22 25 26 29 30 31 34 35 57 58 61 62 65 66 67 70 71
node 3 size: 193490 MB
node 3 free: 193252 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

(Continued on next page)
## Platform Notes (Continued)

From `/proc/meminfo`
- MemTotal: 791006148 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release* /etc/*version*`
- os-release:
  - NAME="SLES"
  - VERSION="15"
  - VERSION_ID="15"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15"
  - ID="sles"
  - ID_LIKE="suse"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:15"

```
uname -a:
Linux linux-db10 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

kernel self-reported vulnerability status:

- CVE-2017-5754 (Meltdown): Not affected
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 4 14:45

SPEC is set to: /home/cpu2017
- Filesystem Type Size Used Avail Use% Mounted on
  - /dev/sda2 btrfs 222G 52G 170G 24% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
- Memory:
  - 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
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Compiler Version Notes

==============================================================================
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|         | 525.x264_r(base) 557.xz_r(base)                     |
|         | Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
|         | Version 19.0.4.227 Build 20190416 |</p>
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</tr>
<tr>
<td></td>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,</td>
</tr>
<tr>
<td></td>
<td>Version 19.0.4.227 Build 20190416</td>
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Base Compiler Invocation

C benchmarks:
  icc -m64 -std=c11

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64

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- 523.xalanbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
- 525.x264_r: -DSPEC_LP64  
- 531.deepsjeng_r: -DSPEC_LP64  
- 541.leela_r: -DSPEC_LP64  
- 548.exchange2_r: -DSPEC_LP64  
- 557.xz_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**

- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
- `-lqkmalloc`

**C++ benchmarks:**

- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
- `-lqkmalloc`

**Fortran benchmarks:**

- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-nostandard-realloc-lhs -align array 32 byte`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
- `-lqkmalloc`

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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