Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5220S, 2.70GHz)

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**Hardware**

- **CPU Name:** Intel Xeon Gold 5220S
- **Max MHz:** 3900
- **Nominal:** 2700
- **Enabled:** 36 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 24.75 MB I+D on chip per chip
- **Cache:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
- **Storage:** 1 x 600G SAS 10K RPM
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --
Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 5220S, 2.70GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 191
SPECrate®2017_fp_peak = Not Run

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NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
umactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5220S, 2.70GHz)

SPECrates
SPECrater®2017_fp_base = 191
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-k1c6 Wed Sep 11 10:13:56 2019
SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5220S CPU @ 2.70GHz
  2. "physical id"s (chips)
    72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
    siblings : 36
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 2
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5220S CPU @ 2.70GHz
Stepping: 7

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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5220S, 2.70GHz)

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### Platform Notes (Continued)

- CPU MHz: 2700.000
- CPU max MHz: 3900.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 5400.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 25344K
- NUMA node0 CPU(s): 0-2,5,6,9,10,14,15,36-38,41,42,45,46,50,51
- NUMA node1 CPU(s): 3,4,7,8,11-13,16,17,39,40,43,44,47-49,52,53
- NUMA node2 CPU(s): 18-20,23,24,27,28,32,33,54-56,59,60,63,64,68,69
- NUMA node3 CPU(s): 21,22,25,26,29-31,34,35,57,58,61,62,65-67,70,71
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
  
  pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rtldscpl
  
  lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
  
  aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
  
  sdbg fma cx16 xtpred pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
  
  tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault
  
  epb cat_l3 cdp_l3 invpcid_single intel_pmm tpr_shadow vmm任教 flexpriority ept
  
  vpid fsgsbase tsc_adjust bni hle avx2 smep bmi2 ernes invpcid rtm cqm mpx rdt_a
  
  avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
  
  xsaveopt xsavec xsavec xvasm cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
  
  ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
  
  ospke avx512_vnni arch_capabilities ssbd

```
//proc/cpuinfo cache data
  cache size : 25344 KB
```

**WARNING:** a numactl 'node' might or might not correspond to a physical chip.

```
numactl --hardware
```

- available: 4 nodes (0-3)
- node 0 cpus: 0 1 2 5 6 9 10 14 15 36 37 38 41 42 45 46 50 51
- node 0 size: 191903 MB
- node 0 free: 186091 MB
- node 1 cpus: 3 4 7 8 11 12 13 16 17 39 40 43 44 47 48 49 52 53
- node 1 size: 193522 MB
- node 1 free: 189500 MB
- node 2 cpus: 18 19 20 23 24 27 28 32 33 54 55 56 59 60 63 64 68 69
- node 2 size: 193522 MB
- node 2 free: 189470 MB
- node 3 cpus: 21 22 25 26 29 30 31 34 35 57 58 61 62 65 66 67 70 71
- node 3 size: 193519 MB
- node 3 free: 189490 MB
- node distances:
  - node 0 1 2 3
  - 0: 10 11 21 21

(Continued on next page)
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Cisco UCS B200 M5 (Intel Xeon Gold 5220S, 2.70GHz)
Cisco Systems
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SPECrater®2017_fp_peak = Not Run

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Test Sponsor: Cisco Systems
Test Date: Aug-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
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<th>C++, C</th>
<th>511.povray_r(base) 526.blender_r(base)</th>
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<th>Fortran</th>
<th>503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)</th>
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<th>Fortran, C</th>
<th>521.wrf_r(base) 527.cam4_r(base)</th>
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Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 5220S, 2.70GHz)

SPECrate®2017_fp_base = 191
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.ibm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64

(Continued on next page)
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Software Availability: May-2019

Base Portability Flags (Continued)
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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