Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6262V, 1.90GHz)

<table>
<thead>
<tr>
<th>Copy</th>
<th>SPEC CPU2017 Floating Point Rate Result</th>
<th>SPEC CPU2017 License</th>
<th>Test Date:</th>
<th>Hardware Availability:</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>96</td>
<td>2017_fp_base = 208</td>
<td>Aug-2019</td>
<td>Apr-2019</td>
</tr>
<tr>
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<td>96</td>
<td>2017_fp_base = 208</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>96</td>
<td>2017_fp_base = 208</td>
<td></td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td>96</td>
<td>2017_fp_base = 208</td>
<td></td>
<td></td>
</tr>
<tr>
<td>511.povray_r</td>
<td>96</td>
<td>2017_fp_base = 208</td>
<td></td>
<td></td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>96</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>96</td>
<td>2017_fp_base = 208</td>
<td></td>
<td></td>
</tr>
<tr>
<td>526.blender_r</td>
<td>96</td>
<td>2017_fp_base = 208</td>
<td></td>
<td></td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>96</td>
<td>2017_fp_base = 208</td>
<td></td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>96</td>
<td>2017_fp_base = 208</td>
<td></td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td>96</td>
<td>2017_fp_base = 208</td>
<td></td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>96</td>
<td>2017_fp_base = 208</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>96</td>
<td>2017_fp_base = 208</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 6262V
- **Max MHz:** 3600
- **Nominal:** 1900
- **Enabled:** 48 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 33 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --
SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6262V, 1.90GHz)

SPECrate®2017_fp_base = 208
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>96</td>
<td>2187</td>
<td>440</td>
<td>2188</td>
<td>440</td>
<td>2187</td>
<td>440</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>96</td>
<td>659</td>
<td>184</td>
<td>656</td>
<td>185</td>
<td>656</td>
<td>185</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>508.namd_r</td>
<td>96</td>
<td>513</td>
<td>178</td>
<td>517</td>
<td>176</td>
<td>512</td>
<td>178</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td>96</td>
<td>2351</td>
<td>107</td>
<td>2355</td>
<td>107</td>
<td>2363</td>
<td>106</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>511.povray_r</td>
<td>96</td>
<td>859</td>
<td>261</td>
<td>863</td>
<td>260</td>
<td>865</td>
<td>259</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>96</td>
<td>935</td>
<td>108</td>
<td>936</td>
<td>108</td>
<td>935</td>
<td>108</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>96</td>
<td>1128</td>
<td>191</td>
<td>1110</td>
<td>194</td>
<td>1121</td>
<td>192</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>526.blender_r</td>
<td>96</td>
<td>583</td>
<td>251</td>
<td>584</td>
<td>251</td>
<td>583</td>
<td>251</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>96</td>
<td>636</td>
<td>264</td>
<td>630</td>
<td>266</td>
<td>634</td>
<td>265</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>96</td>
<td>431</td>
<td>554</td>
<td>430</td>
<td>555</td>
<td>430</td>
<td>555</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td>96</td>
<td>416</td>
<td>388</td>
<td>416</td>
<td>388</td>
<td>417</td>
<td>387</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>96</td>
<td>2623</td>
<td>143</td>
<td>2624</td>
<td>143</td>
<td>2624</td>
<td>143</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>96</td>
<td>1848</td>
<td>82.5</td>
<td>1862</td>
<td>81.9</td>
<td>1850</td>
<td>82.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

PECrate®2017_fp_base = 208
PECrate®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = ":/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6262V, 1.90GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrater®2017_fp_base = 208
SPECrater®2017_fp_peak = Not Run

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-pmqx Wed Sep 4 20:19:19 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6262V CPU @ 1.90GHz
  2  "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6262V, 1.90GHz)
Platform Notes (Continued)

node  0  1  2  3
0:  10 11 21 21
1:  11 10 21 21
2:  21 21 10 11
3:  21 21 11 10

From /proc/meminfo
MemTotal: 791164568 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PPRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-pmqx 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Sep 4 14:47

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb4 btrfs 169G 35G 134G 21% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
   24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

================================================================================
C | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)

(Continued on next page)
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</table>

Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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C++

| 508.namd_r(base) 510.parest_r(base) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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C++, C

| 511.povray_r(base) 526.blender_r(base) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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C++, C, Fortran

| 507.cactuBSSN_r(base) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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Fortran

| 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base) |

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
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(Continued on next page)
Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6262V, 1.90GHz)

SPECrate®2017_fp_base = 208
SPECrate®2017_fp_peak = Not Run

Compiler Version Notes (Continued)

Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.ibm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

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Cisco UCS B200 M5 (Intel Xeon Gold 6262V, 1.90GHz)

SPECRate®2017_fp_base = 208
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CPU2017 License: 9019
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Base Portability Flags (Continued)

544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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## Cisco Systems

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</tr>
</thead>
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Originally published on 2019-10-01.