## CPU Specifications

**CPU Name:** Intel Xeon Gold 6222V  
**Max MHz:** 3600  
**Nominal:** 1800  
**Enabled:** 40 cores, 2 chips, 2 threads/core  
**Orderable:** 1,2 Chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**Cache L2:** 1 MB I+D on chip per core  
**Cache L3:** 27.5 MB I+D on chip per chip  
**Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)  
**Storage:** 1 x 1.9 TB SSD SAS  
**Other:** None

## Software Specifications

**OS:** SUSE Linux Enterprise Server 15 (x86_64)  
**4.12.14-23-default**  
**Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
**Fortran:** Version 19.0.4.227 of Intel Fortran Compiler for Linux  
**Parallel:** No  
**Firmware:** Version 4.0.4b released Apr-2019  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** Not Applicable

## Test Details

- **CPU2017 License:** 9019  
- **Test Sponsor:** Cisco Systems  
- **Test Date:** Aug-2019  
- **Hardware Availability:** Apr-2019  
- **Tested by:** Cisco Systems  
- **Software Availability:** May-2019  
- **Tested by:** Cisco Systems  
- **Software Availability:** May-2019

## Results

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<th>SPECrate®2017_int_peak</th>
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<td>548.exchange2_r</td>
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<td>557.xz_r</td>
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**Cisco Systems**  
Cisco UCS B200 M5 (Intel Xeon Gold 6222V, 1.80GHz)  

**SPECrater®2017_int_base = 201**  
**SPECrater®2017_int_peak = Not Run**
SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6222V, 1.80GHz)

SPECraten®2017_int_base = 201
SPECraten®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

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<td>150</td>
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</tbody>
</table>

SPECraten®2017_int_base = 201
SPECraten®2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
   sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
   numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6222V, 1.80GHz)

SPECrater®2017_int_base = 201
SPECrater®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-aixk Wed Sep 4 15:08:34 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6222V CPU @ 1.80GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
```

From lscpu:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6222V CPU @ 1.80GHz
Stepping: 7
CPU MHz: 1800.000
```

(Continued on next page)
## Platform Notes (Continued)

| CPU max MHz: | 3600.0000 |
| CPU min MHz: | 800.0000 |
| BogoMIPS: | 3600.00 |
| Virtualization: | VT-x |
| L1d cache: | 32K |
| L1i cache: | 32K |
| L2 cache: | 1024K |
| L3 cache: | 28160K |
| NUMA node0 CPU(s): | 0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56 |
| NUMA node1 CPU(s): | 3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59 |
| NUMA node2 CPU(s): | 20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76 |
| NUMA node3 CPU(s): | 23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79 |
| Flags: | fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdseed lahf_lm abm 3dnowprefetch cpuid_fault ebp cat_l3 cdp_l3 invpcid_single intel_p6in mba tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local ibpb ibrs tsodi dhpmr ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pkuk ospke avx512_vnni arch_capabilities ssbd |

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

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<thead>
<tr>
<th>node</th>
<th>cpus</th>
<th>size</th>
<th>free</th>
</tr>
</thead>
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<tr>
<td>0</td>
<td>0-1</td>
<td>192090 MB</td>
<td>191805 MB</td>
</tr>
<tr>
<td>1</td>
<td>3-7</td>
<td>193521 MB</td>
<td>193010 MB</td>
</tr>
<tr>
<td>2</td>
<td>20-22</td>
<td>193492 MB</td>
<td>193244 MB</td>
</tr>
<tr>
<td>3</td>
<td>23-29</td>
<td>193519 MB</td>
<td>193288 MB</td>
</tr>
<tr>
<td>node distances:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0: 1 1 2 3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1: 11 10 21 21</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6222V, 1.80GHz)

SPECRate®2017_int_base = 201
SPECRate®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2019
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Software Availability: May-2019

Platform Notes (Continued)

2:  21  21  10  11
3:  21  21  11  10

From /proc/meminfo
MemTotal:       791167644 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-aixk 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Sep 4 14:45

SPEC is set to: /home/cpu2017
  Filesystem  Type  Size  Used Avail Use% Mounted on
  /dev/sdb6      xfs    45G   13G   33G  28% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
  Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
|     | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) |
|     | 525.x264_r(base) 557.xz_r(base)     |
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6222V, 1.80GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------
C++ | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
    | 541.leela_r(base)
-----------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------
Fortran | 548.exchange2_r(base)
-----------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64

(Continued on next page)
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Base Portability Flags (Continued)
557.xz_r: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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