Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Gold 6262V</td>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
</tr>
<tr>
<td>Max MHz: 3600</td>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Nominal: 1900</td>
<td>Parallel: No</td>
</tr>
<tr>
<td>Enabled: 48 cores, 2 chips, 2 threads/core</td>
<td>Firmware: Version 4.0.4g released Jul-2019</td>
</tr>
<tr>
<td>Orderable: 1.2 Chips</td>
<td>File System: xfs</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>L2: 1 MB I+D on chip per core</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>L3: 33 MB I+D on chip per chip</td>
<td>Peak Pointers: 32/64-bit</td>
</tr>
<tr>
<td>Other: None</td>
<td>Other: jemalloc memory allocator V5.0.1</td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)</td>
<td>Power Management: --</td>
</tr>
<tr>
<td>Storage: 1 x 1.9 TB SSD SAS</td>
<td></td>
</tr>
</tbody>
</table>

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

<table>
<thead>
<tr>
<th>Test Date: Sep-2019</th>
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<tbody>
<tr>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Software Availability: May-2019</td>
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<tr>
<td>502.gcc_r</td>
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<td>505.mcf_r</td>
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<tr>
<td>520.omnetpp_r</td>
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<tr>
<td>523.xalancbmk_r</td>
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<tr>
<td>525.x264_r</td>
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<tr>
<td>531.deepsjeng_r</td>
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</tr>
<tr>
<td>541.leela_r</td>
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<tr>
<td>548.exchange2_r</td>
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<td>557.xz_r</td>
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Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

Cisco Systems

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

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</tr>
</tbody>
</table>

SPECrate®2017_int_base = 244
SPECrate®2017_int_peak = 255

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

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<tr>
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</table>

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<th>9019</th>
</tr>
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<td>Test Sponsor</td>
<td>Cisco Systems</td>
</tr>
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<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date</td>
<td>Sep-2019</td>
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<td>Hardware Availability</td>
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</tbody>
</table>

General Notes (Continued)

is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcede8f2999c33d61f64985e45859ea9
running on linux-ylla Thu Sep 19 00:03:48 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6262V CPU @ 1.90GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
```

From lscpu:

```
Architecture:       x86_64
CPU op-mode(s):     32-bit, 64-bit
Byte Order:         Little Endian
CPU(s):             96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s):          2
NUMA node(s):       4
Vendor ID:          GenuineIntel
CPU family:         6
Model:              85
Model name:         Intel(R) Xeon(R) Gold 6262V CPU @ 1.90GHz
Stepping:           7
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

CPU MHz: 1900.000
CPU max MHz: 3600.0000
CPU min MHz: 800.0000
BogoMIPS: 3800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 33792K
NUMA node0 CPU(s): 0-2, 6-8, 12-14, 18-20, 24-26, 30-32, 36-38, 42-44, 47-50, 54-56, 60-62, 66-68
NUMA node1 CPU(s): 27-29, 33-35, 39-41, 45-47, 72-74, 78-80, 84-86, 90-92
NUMA node3 CPU(s): 3-5, 9-11, 15-17, 21-23, 27-29, 33-35, 39-41, 45-47, 72-74, 78-80, 84-86, 90-92

Flags:
          fpu    vme    de     pse    tsc    msr    pae     mce    cx8    apic   sep
          mtrr  pge     mca    cmov  pat    pse36  c10flush  dtc  acpi   movbe
          popcnt
          tsc_deadline_timer
          aes
          xsave
          avx
          f16c
          rdrand
          lahf_lm
          abm
          3dnowprefetch
          cpuid_fault
          epb
          cat
          cdp
          l3
          invpcid_single
          intel_ppackage
          mba
          tpr_shadow
          cpuid_fault
          ssbd

From numacl --hardware
WARNING: a numacl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 12 13 14 18 19 20 48 49 50 54 55 56 60 61 62 66 68
node 0 size: 192102 MB
node 0 free: 191764 MB
node 1 cpus: 3 4 5 9 10 11 15 16 17 21 22 23 51 52 53 57 58 59 63 64 65 69 70 71
node 1 size: 193497 MB
node 1 free: 193214 MB
node 2 cpus: 24 25 26 30 31 32 36 37 38 42 43 44 47 72 73 74 78 79 80 84 85 86 90 91 92
node 2 size: 193526 MB
node 2 free: 193080 MB
node 3 cpus: 27 28 29 33 34 35 39 40 41 45 46 47 75 76 77 81 82 83 87 88 89 93 94 95
node 3 size: 193523 MB
node 3 free: 193303 MB
node distances:
node 0 1 2 3
0: 10 11 21 21

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

| SPECrate\textsuperscript{®}2017 int_base | 244 |
| SPECrate\textsuperscript{®}2017 int_peak | 255 |

| CPU2017 License: | 9019 |
| Test Date: | Sep-2019 |
| Test Sponsor: | Cisco Systems |
| Test Date: | Sep-2019 |
| Tested by: | Cisco Systems |
| Hardware Availability: | Apr-2019 |
| Software Availability: | May-2019 |

**Platform Notes (Continued)**

1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From `/proc/meminfo`
- MemTotal: 791192984 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release*/etc/*version*`
- os-release:
  - NAME="SLES"
  - VERSION="15"
  - VERSION_ID="15"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15"
  - ID="sles"
  - ID_LIKE="suse"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
- Linux linux-ylla 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
- x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 18 23:58

SPEC is set to: /home/cpu2017

**Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.**

BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019

Memory:
- 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

SPECrate®2017_int_base = 244
SPECrate®2017_int_peak = 255

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C++     | 523.xalancbmk_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

SPECrater®2017_int_base = 244
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CPU2017 License: 9019
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Software Availability: May-2019

Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------

C++ | 523.xalancbmk_r(peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Fortran | 548.exchange2_r(base, peak)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

(Continued on next page)
## Cisco Systems

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

---

### Base Portability Flags (Continued)

- `502.gcc_r`: `-DSPEC_LP64`
- `505.mcf_r`: `-DSPEC_LP64`
- `520.omnetpp_r`: `-DSPEC_LP64`
- `523.xalancbmk_r`: `-DSPEC_LP64`  
- `525.x264_r`: `-DSPEC_LP64`
- `531.deepsjeng_r`: `-DSPEC_LP64`
- `541.leela_r`: `-DSPEC_LP64`
- `548.exchange2_r`: `-DSPEC_LP64`
- `557.xz_r`: `-DSPEC_LP64`

### Base Optimization Flags

**C benchmarks:**

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

**C++ benchmarks:**

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

**Fortran benchmarks:**

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

---

### Peak Compiler Invocation

**C benchmarks (except as noted below):**

```
icc -m64 -std=c11
```

```
```

**C++ benchmarks (except as noted below):**

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

(Continued on next page)
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Test Sponsor: Cisco Systems
Test Date: Sep-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Fortran benchmarks:
ifort -m64

Peak Compiler Invocation (Continued)

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
502.gcc_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc
505.mcf_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
525.x264_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
557.xz_r: Same as 505.mcf_r

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)  

| SPECrate®2017 int_base = 244 |
| SPECrate®2017 int_peak = 255 |

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Sep-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

Peak Optimization Flags (Continued)

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-L/usr/local/jemalloc -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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