Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

SPECrate®2017_int_base = 244
SPECrate®2017_int_peak = 255

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++
Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran
Compiler for Linux
Parallel: No
Firmware: Version 4.0.4g released Jul-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: --

Hardware
CPU Name: Intel Xeon Gold 6262V
Max MHz: 3600
Nominal: 1900
Enabled: 48 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 33 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

500.perlbench_r 96
502.gcc_r 96
505.mcf_r 96
520.omnetpp_r 96
523.xalancbmk_r 96
525.x264_r 96
531.deepsjeng_r 96
541.leela_r 96
548.exchange2_r 96
557.xz_r 96

500.perlbench_r
502.gcc_r
505.mcf_r
520.omnetpp_r
523.xalancbmk_r
525.x264_r
531.deepsjeng_r
541.leela_r
548.exchange2_r
557.xz_r

SPECrate®2017_int_base (244)
SPECrate®2017_int_peak (255)
**SPEC CPU®2017 Integer Rate Result**

**Cisco Systems**

Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

**Copyright 2017-2020 Standard Performance Evaluation Corporation**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
<td>822</td>
<td>186</td>
<td>818</td>
<td>187</td>
<td>818</td>
<td>187</td>
<td>96</td>
<td>706</td>
<td>217</td>
<td>704</td>
<td>217</td>
<td>706</td>
<td>217</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>96</td>
<td>698</td>
<td>195</td>
<td>690</td>
<td>197</td>
<td>701</td>
<td>194</td>
<td>96</td>
<td>587</td>
<td>231</td>
<td>590</td>
<td>230</td>
<td>590</td>
<td>231</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>96</td>
<td>498</td>
<td>311</td>
<td>499</td>
<td>311</td>
<td>498</td>
<td>312</td>
<td>96</td>
<td>499</td>
<td>311</td>
<td>497</td>
<td>312</td>
<td>498</td>
<td>311</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>96</td>
<td>787</td>
<td>160</td>
<td>786</td>
<td>160</td>
<td>787</td>
<td>160</td>
<td>96</td>
<td>788</td>
<td>160</td>
<td>787</td>
<td>160</td>
<td>786</td>
<td>160</td>
</tr>
<tr>
<td>523.xalanbfmk_r</td>
<td>96</td>
<td>394</td>
<td>258</td>
<td>394</td>
<td>258</td>
<td>393</td>
<td>258</td>
<td>96</td>
<td>362</td>
<td>280</td>
<td>362</td>
<td>280</td>
<td>362</td>
<td>280</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>96</td>
<td>330</td>
<td>510</td>
<td>328</td>
<td>512</td>
<td>327</td>
<td>514</td>
<td>96</td>
<td>314</td>
<td>536</td>
<td>313</td>
<td>538</td>
<td>314</td>
<td>536</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>96</td>
<td>540</td>
<td>204</td>
<td>540</td>
<td>204</td>
<td>540</td>
<td>204</td>
<td>96</td>
<td>540</td>
<td>204</td>
<td>539</td>
<td>204</td>
<td>540</td>
<td>204</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>96</td>
<td>853</td>
<td>186</td>
<td>835</td>
<td>190</td>
<td>835</td>
<td>190</td>
<td>96</td>
<td>846</td>
<td>188</td>
<td>836</td>
<td>190</td>
<td>845</td>
<td>188</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>96</td>
<td>513</td>
<td>490</td>
<td>513</td>
<td>490</td>
<td>513</td>
<td>490</td>
<td>96</td>
<td>513</td>
<td>490</td>
<td>514</td>
<td>489</td>
<td>513</td>
<td>490</td>
</tr>
<tr>
<td>557.nnz_r</td>
<td>96</td>
<td>624</td>
<td>166</td>
<td>624</td>
<td>166</td>
<td>624</td>
<td>166</td>
<td>96</td>
<td>624</td>
<td>166</td>
<td>624</td>
<td>166</td>
<td>625</td>
<td>166</td>
</tr>
</tbody>
</table>

**Results Table**

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**General Notes**

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

testrun = "sync; echo 3 > /proc/sys/vm/drop_caches"
	estrun command invoked through numactl i.e.:

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>244</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>255</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Sep-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

**General Notes (Continued)**

is mitigated in the system as tested and documented.  
jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  

**Platform Notes**

BIOS Settings:
Intel HyperThreading Technology set to Enabled  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9  
running on linux-ylla Thu Sep 19 00:03:48 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6262V CPU @ 1.90GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
  siblings : 48
  physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
  physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
```

From lscpu:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6262V CPU @ 1.90GHz
Stepping: 7
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

<table>
<thead>
<tr>
<th>CPU MHz:</th>
<th>1900.000</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU max MHz:</td>
<td>3600.0000</td>
</tr>
<tr>
<td>CPU min MHz:</td>
<td>800.0000</td>
</tr>
<tr>
<td>BogoMIPS:</td>
<td>3800.00</td>
</tr>
<tr>
<td>Virtualization:</td>
<td>VT-x</td>
</tr>
<tr>
<td>L1d cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L1i cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache:</td>
<td>1024K</td>
</tr>
<tr>
<td>L3 cache:</td>
<td>33792K</td>
</tr>
</tbody>
</table>

**NUMA node0 CPU(s):** 0-2, 6-8, 12-14, 18-20, 48-50, 54-56, 60-62, 66-68  
**NUMA node1 CPU(s):** 3-5, 9-11, 15-17, 21-23, 51-53, 57-59, 63-65, 69-71  
**NUMA node2 CPU(s):** 24-26, 30-32, 36-38, 42-44, 72-74, 78-80, 84-86, 90-92  
**NUMA node3 CPU(s):** 27-29, 33-35, 39-41, 45-47, 75-77, 81-83, 87-89, 93-95

**Flags:**  
fpum vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov  
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp  
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid  
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3  
sdbg fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt  
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault  
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vmmi flexpriority ept  
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2  
ems invpcid rtm cqm mpx rdt_a axv512f axv512d rdseed adx smap clflushopt clwb intel_pt  
avx512cd avx512bw avx512vl xsavesopt xsavec xgetbv1 xsave vmm vncq_curregar vncq_curreg  
cqmm debug_host vncq_host vncq_vncreg vncq_vncreg vncq_vncreg vncq_vncreg vncq_vncreg vncq_vncreg

/proc/cpuinfo cache data  
cache size : 33792 KB

From numactl --hardware  
WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)  
node 0 cpus: 0 1 2 6 7 8 12 13 14 18 19 20 48 49 50 54 55 56 60 61 62 66 67 68  
node 0 size: 192102 MB  
node 0 free: 191764 MB  
node 1 cpus: 3 4 5 9 10 11 15 16 17 21 22 23 51 52 53 57 58 59 63 64 65 69 70 71  
node 1 size: 193497 MB  
node 1 free: 193214 MB  
node 2 cpus: 24 25 26 30 31 32 36 37 38 42 43 44 72 73 74 76 77 81 82 83 87 88 89 93 94 95  
node 2 size: 193526 MB  
node 2 free: 193080 MB  
node 3 cpus: 27 28 29 33 34 35 39 40 41 45 46 47 75 76 77 81 82 83 87 88 89 93 94 95  
node 3 size: 193523 MB  
node 3 free: 193303 MB  
node distances:  
node 0 1 2 3  
0: 10 11 21 21

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

SPECrate®2017_int_base = 244
SPECrate®2017_int_peak = 255

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791192984 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-ylla 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 18 23:58
SPEC is set to: /home/cpu2017

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)
## Compiler Version Notes

<table>
<thead>
<tr>
<th>Language</th>
<th>Test Cases</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>502.gcc_r(peak)</td>
</tr>
<tr>
<td>Intel(R) C</td>
<td>Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
</tr>
<tr>
<td>C</td>
<td>500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)</td>
</tr>
<tr>
<td>Intel(R) C</td>
<td>Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
</tr>
<tr>
<td>C++</td>
<td>523.xalancbmk_r(peak)</td>
</tr>
<tr>
<td>Intel(R) C++</td>
<td>Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
</tr>
<tr>
<td>C++</td>
<td>520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)</td>
</tr>
<tr>
<td>Intel(R) C++</td>
<td>Intel(R) 64 Compiler for applications running on Intel(R) 64,</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

 SPECrate®2017_int_base = 244
 SPECrate®2017_int_peak = 255

CPU2017 License: 9019
Test Date: Sep-2019
Test Sponsor: Cisco Systems
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: May-2019

Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++     | 523.xalancbmk_r(peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
        | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 548.exchange2_r(base, peak)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz) | SPECrate®2017_int_base = 244
SPECrate®2017_int_peak = 255

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Portability Flags (Continued)

502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>244</td>
<td>255</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Fortran benchmarks:
ifort -m64

Peak Compiler Invocation (Continued)

Peak Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags
C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6262V, 1.90GHz)

SPECrate\textsuperscript{®}2017\_int\_base = 244  
SPECrate\textsuperscript{®}2017\_int\_peak = 255

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

### Peak Optimization Flags (Continued)

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-L/usr/local/jemalloc-5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

---

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU\textsuperscript{®}2017 v1.0.5 on 2019-09-19 03:03:47-0400.  
Originally published on 2019-11-04.