## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5215, 2.50GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64)</td>
<td>CPU Name: Intel Xeon Gold 5215</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
<td>Max MHz: 3400</td>
</tr>
<tr>
<td>Firmware: Version 4.0.4g released Jul-2019</td>
<td>Nominal: 2500</td>
</tr>
<tr>
<td>File System: xfs</td>
<td>Enabled: 20 cores, 2 chips</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Orderable: 1.2 Chips</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Peak Pointers: 64-bit</td>
<td>L2: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>Other: None</td>
<td>L3: 13.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Power Management: --</td>
<td>Other: None</td>
</tr>
</tbody>
</table>

### SPEC CPU 2017 Floating Point Speed Result

<table>
<thead>
<tr>
<th>Test Date: Sep-2019</th>
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<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2019</td>
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<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
<tr>
<td>CPU2017 License: 9019</td>
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### SPECspeed®2017_fp_base = 90.7

### SPECspeed®2017_fp_peak = 91.1

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<thead>
<tr>
<th>SPECspeed®2017_fp_base = 90.7</th>
<th>SPECspeed®2017_fp_peak (91.1)</th>
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<tbody>
<tr>
<td>Threads</td>
<td>SPECspeed®2017_fp_base (90.7)</td>
</tr>
<tr>
<td>603.bwaves_s 20</td>
<td>98.2</td>
</tr>
<tr>
<td>607.cactuBSSN_s 20</td>
<td>97.8</td>
</tr>
<tr>
<td>619.lbm_s 20</td>
<td>76.8</td>
</tr>
<tr>
<td>621.wrf_s 20</td>
<td>84.4</td>
</tr>
<tr>
<td>627.cam4_s 20</td>
<td>52.5</td>
</tr>
<tr>
<td>628.pop2_s 20</td>
<td>66.1</td>
</tr>
<tr>
<td>638.imagick_s 20</td>
<td>122</td>
</tr>
<tr>
<td>644.nab_s 20</td>
<td>70.2</td>
</tr>
<tr>
<td>649.fotonik3d_s 20</td>
<td>70.2</td>
</tr>
<tr>
<td>654.roms_s 20</td>
<td>83.0</td>
</tr>
</tbody>
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### SPECspeed®2017_fp_peak (91.1)

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### SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS C220 M5 (Intel Xeon Gold 5215, 2.50GHz)

### SPECspeed®2017_fp_base = 90.7

**SPECspeed®2017_fp_peak = 91.1**

---

**Results Table**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Base</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Base</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Base</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Base</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>20</td>
<td>153</td>
<td>386</td>
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<td>153</td>
<td>385</td>
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<td>154</td>
<td>383</td>
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<td>155</td>
<td>381</td>
<td>154</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>20</td>
<td>170</td>
<td>97.8</td>
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<td>170</td>
<td>98.3</td>
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<td>170</td>
<td>98.2</td>
<td></td>
<td>171</td>
<td>98.6</td>
<td>170</td>
</tr>
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<td>76.6</td>
<td></td>
<td>68.6</td>
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<td>75.6</td>
<td></td>
<td>68.1</td>
<td>76.9</td>
<td>68.3</td>
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<tr>
<td>621.wrf_s</td>
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<td>83.8</td>
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<td>157</td>
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<td>157</td>
<td>84.4</td>
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<td>152</td>
<td>87.2</td>
<td>151</td>
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<td>627.cam4_s</td>
<td>20</td>
<td>169</td>
<td>52.3</td>
<td></td>
<td>169</td>
<td>52.5</td>
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<td>169</td>
<td>52.5</td>
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<td>191</td>
<td>62.3</td>
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<td>187</td>
<td>63.4</td>
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<td>20</td>
<td>218</td>
<td>66.1</td>
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</tr>
<tr>
<td>644.nab_s</td>
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<td>143</td>
<td>122</td>
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<td></td>
<td>143</td>
<td>122</td>
<td>143</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
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<td>130</td>
<td>70.2</td>
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<td>130</td>
<td>70.2</td>
<td></td>
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<td>70.2</td>
<td></td>
<td>130</td>
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<td>130</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>20</td>
<td>190</td>
<td>82.8</td>
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<td>189</td>
<td>83.4</td>
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<td>83.0</td>
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<td>83.3</td>
<td>189</td>
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**SPECspeed®2017_fp_base = 90.7**

**SPECspeed®2017_fp_peak = 91.1**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "~/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

- BIOS Settings:
  - Intel HyperThreading Technology set to Disabled
  - CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5215, 2.50GHz)

SPEC CPU®2017 Floating Point Speed Result

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SPECspeed®2017_fp_base = 90.7
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Sep-2019
Hardware Availability: Apr-2019
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Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-bo7k Mon Sep 23 04:07:42 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 5215 CPU @ 2.50GHz
    2  "physical id"s (chips)
    20  "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 10
    siblings : 10
    physical 0: cores 0 1 2 3 4 8 9 10 11 12
    physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
    Architecture: x86_64
    CPU op-mode(s): 32-bit, 64-bit
    Byte Order: Little Endian
    CPU(s): 20
    On-line CPU(s) list: 0-19
    Thread(s) per core: 1
    Core(s) per socket: 10
    Socket(s): 2
    NUMA node(s): 2
    Vendor ID: GenuineIntel
    CPU family: 6
    Model: 85
    Model name: Intel(R) Xeon(R) Gold 5215 CPU @ 2.50GHz
    Stepping: 6
    CPU MHz: 2500.000
    CPU max MHz: 3400.0000
    CPU min MHz: 1000.0000
    BogoMIPS: 5000.00
    Virtualization: VT-x
    L1d cache: 32K
    L1i cache: 32K
    L2 cache: 1024K
    L3 cache: 14080K
    NUMA node0 CPU(s): 0-9

(Continued on next page)
Cisco Systems
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CPU2017 License: 9019
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Tested by: Cisco Systems
Test Date: Sep-2019
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Platform Notes (Continued)

NUMA node1 CPU(s): 10-19
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfprof tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
eb cat_id cpd_id invpcid_single intel_patin mba tpr_shadow vmni flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cmq mxp rdrt_a
avx512f avx512dq rdseed adx xsaveopt xsaves xsaveopt xgetbv1 xsaves cmq_llc cmq_occupa_llc cmq_mbmax_total

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9
node 0 size: 385605 MB
node 0 free: 385105 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19
node 1 size: 387058 MB
node 1 free: 379532 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 791207772 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

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SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5215, 2.50GHz)

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Platform Notes (Continued)

uname -a:
    Linux linux-bo7k 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 22 22:51

SPEC is set to: /home/cpu2017
    Filesystem  Type  Size  Used Avail Use% Mounted on
    /dev/sda1    xfs   224G   26G  198G  12% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
    Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)                     |
|                 | 644.nab_s(base, peak)                                                |
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
    Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================

C++, C, Fortran | 607.cactuBSSN_s(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
    Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak)
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Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
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Intel (R) C Intel (R) 64 Compiler for applications running on Intel (R) 64,
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64
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**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Sep-2019  
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### Base Portability Flags

- 603.bwaves_s: -DSPEC_LP64
- 607.cactuBSSN_s: -DSPEC_LP64
- 619.hm_s: -DSPEC_LP64
- 621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl
- 638.imagick_s: -DSPEC_LP64
- 644.nab_s: -DSPEC_LP64
- 649.fotonik3d_s: -DSPEC_LP64
- 654.roms_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

**Fortran benchmarks:**

-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

**Benchmarks using both Fortran and C:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

**Benchmarks using Fortran, C, and C++:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

### Peak Compiler Invocation

**C benchmarks:**

icc -m64 -std=c11

**Fortran benchmarks:**

ifort -m64

(Continued on next page)
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Peak Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:

603.bwaves_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4
-qopenmp -nostandard-realloc-lhs

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-qopenmp -nostandard-realloc-lhs

Benchmarks using both Fortran and C:

621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs

628.pop2_s: Same as 621.wrf_s

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5215, 2.50GHz)

SPECbw®2017_fp_base = 90.7
SPECbw®2017_fp_peak = 91.1

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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