Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4210, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Specspeed®2017_int_base = 8.09
Specspeed®2017_int_peak = Not Run

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>0.0</th>
<th>1.0</th>
<th>2.0</th>
<th>3.0</th>
<th>4.0</th>
<th>5.0</th>
<th>6.0</th>
<th>7.0</th>
<th>8.0</th>
<th>9.0</th>
<th>10.0</th>
<th>11.0</th>
<th>12.0</th>
<th>13.0</th>
<th>14.0</th>
<th>15.0</th>
<th>16.0</th>
<th>17.0</th>
<th>18.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>20</td>
<td>5.52</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td>7.88</td>
<td></td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>20</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>10.5</td>
<td></td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>20</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>10.2</td>
<td></td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>20</td>
<td>5.14</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11.4</td>
<td></td>
</tr>
<tr>
<td>625.x264_s</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.60</td>
<td></td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.92</td>
<td></td>
</tr>
<tr>
<td>641.leela_s</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>20</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td>13.7</td>
<td></td>
</tr>
<tr>
<td>657.xz_s</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

--- SPECspeed®2017_int_base (8.09) ---

Hardware

CPU Name: Intel Xeon Silver 4210
Max MHz: 3200
Nominal: 2200
Enabled: 20 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 13.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64)
4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++
Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran
Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4g released Jul-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: --
Cisco Systems
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CPU2017 License: 9019
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SPECspeed®2017_int_base = 8.09
SPECspeed®2017_int_peak = Not Run

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>20</td>
<td>322</td>
<td>5.52</td>
<td>321</td>
<td>5.54</td>
<td>324</td>
<td>5.48</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>20</td>
<td>504</td>
<td>7.89</td>
<td>507</td>
<td>7.85</td>
<td>505</td>
<td>7.88</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>20</td>
<td>450</td>
<td>10.5</td>
<td>450</td>
<td>10.5</td>
<td>450</td>
<td>10.5</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>20</td>
<td>317</td>
<td>5.14</td>
<td>317</td>
<td>5.14</td>
<td>319</td>
<td>5.11</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>20</td>
<td>140</td>
<td>10.2</td>
<td>139</td>
<td>10.2</td>
<td>138</td>
<td>10.3</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>20</td>
<td>155</td>
<td>11.4</td>
<td>155</td>
<td>11.4</td>
<td>155</td>
<td>11.4</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>20</td>
<td>312</td>
<td>4.59</td>
<td>312</td>
<td>4.60</td>
<td>311</td>
<td>4.60</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>20</td>
<td>435</td>
<td>3.92</td>
<td>436</td>
<td>3.92</td>
<td>436</td>
<td>3.92</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>20</td>
<td>215</td>
<td>13.7</td>
<td>215</td>
<td>13.7</td>
<td>215</td>
<td>13.7</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>20</td>
<td>348</td>
<td>17.8</td>
<td>348</td>
<td>17.8</td>
<td>348</td>
<td>17.8</td>
</tr>
</tbody>
</table>

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
Cisco Systems
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| SPECspeed®2017_int_base = 8.09 |
| SPECspeed®2017_int_peak = Not Run |

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Sep-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Disabled  
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9  
running on linux-bo7k Wed Sep 25 07:31:19 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
  2 "physical id"s (chips)
  20 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores: 10
  siblings: 10
  physical 0: cores 0 1 2 3 4 8 9 10 11 12
  physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 20
On-line CPU(s) list: 0-19
Thread(s) per core: 1
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
Stepping: 6
CPU MHz: 2200.000
CPU max MHz: 3200.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

(Continued on next page)
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Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9
NUMA node1 CPU(s): 10-19
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vmni flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsavesopt xsavec xgetbv1 xsavec qmm溃疡 qm_mbm_total qm_mbm_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

/pro/proc/cpuinfo cache data
  cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9
  node 0 size: 385634 MB
  node 0 free: 385039 MB
  node 1 cpus: 10 11 12 13 14 15 16 17 18 19
  node 1 size: 387029 MB
  node 1 free: 386649 MB
  node distances:
  node  0  1
  0:  10  21
  1:  21  10

From /proc/meminfo
MemTotal: 791207772 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
**SPEC CPU®2017 Integer Speed Result**

**Cisco Systems**
Cisco UCS C220 M5 (Intel Xeon Silver 4210, 2.20GHz)

<table>
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<th>SPECspeed®2017_int_base = 8.09</th>
</tr>
</thead>
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</tbody>
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**CPU2017 License:** 9019  
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**Platform Notes (Continued)**

```
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-bo7k 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 25 07:30

SPEC is set to: /home/cpu2017
  Filesystem  Type  Size  Used  Avail  Use%  Mounted on
  /dev/sda1      xfs   224G   20G  204G   9%  /
```

Additional information from dmidecode follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Memory: 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400
```

(End of data from sysinfo program)

---

**Compiler Version Notes**

```
C     | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)  
     | 625.x264_s(base) 657.xz_s(base)  

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

```
C++ | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)  
     | 641.leela_s(base)  

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
```

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SPECSpeed®2017_int_base = 8.09
SPECSpeed®2017_int_peak = Not Run

Compiler Version Notes (Continued)
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------
Fortran | 648.exchange2_s(base)
------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

(Continued on next page)
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C benchmarks (continued):
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml