Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8280L, 2.70GHz)

<table>
<thead>
<tr>
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</table>

**Hardware**

- **CPU Name:** Intel Xeon Platinum 8280L
- **Max MHz:** 4000
- **Nominal:** 2700
- **Enabled:** 56 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 38.5 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4g released Jul-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** Jemalloc memory allocator V5.0.1
- **Power Management:** --
**SPEC CPU®2017 Integer Speed Result**

**Cisco Systems**
Cisco UCS C220 M5 (Intel Xeon Platinum 8280L, 2.70GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
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</table>

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**General Notes**

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
Memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
```
sync; echo 3>/proc/sys/vm/drop_caches
```
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8280L, 2.70GHz)

SPEC speed®2017_int_base = 10.7
SPEC speed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcd8f2999c33d6f64985e45859ea9
running on linux-jm4k Fri Sep 20 00:57:02 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8280L CPU @ 2.70GHz
  2 "physical id"s (chips)
  56 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 28
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 56
On-line CPU(s) list: 0-55
Thread(s) per core: 1
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8280L CPU @ 2.70GHz
Stepping: 7
CPU MHz: 2700.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 5400.00
Virtualization: VT-x

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8280L, 2.70GHz)

| SPECspeed®2017_int_base = 10.7 |
| SPECspeed®2017_int_peak = Not Run |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

**Platform Notes (Continued)**

```
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            39424K
NUMA node0 CPU(s):   0-27
NUMA node1 CPU(s):   28-55
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
                     pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
                     lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
                     aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
                     sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
                     tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
                     epb cat_l3 cdp_l3 invpcid_single intel_patin mba tpr_shadow vni flexpriority ept
                     vpid fsgsbase tsc_adjust bndi hle avx2 smep bmi2 erva invpcid rtm cqm mpx rdts_a
                     avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
                     xsaveopt xsave xsavec xcked xstore xstate cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
                     ibpb ibrs stibp dtherm tPA pln pts hwp hwp_act_window hwp_epp hwp_kd_req pku
                     ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
    cache size : 39424 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
    node 0 size: 385637 MB
    node 0 free: 384836 MB
    node 1 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52
                     53 54 55
    node 1 size: 387030 MB
    node 1 free: 386637 MB
    node distances:
    node  0  1
    0: 10 21
    1: 21 10

From /proc/meminfo
    MemTotal:       791212312 kB
    HugePages_Total:       0
    Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
    os-release:
        NAME="SLES"
        VERSION="15"
        VERSION_ID="15"
```

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Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8280L, 2.70GHz)

| SPECspeed®2017_int_base = 10.7 |
| SPECspeed®2017_int_peak = Not Run |

Platform Notes (Continued)

PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-jm4k 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 20 00:52
SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used  Avail Use% Mounted on
/dev/sdb1      xfs  224G  20G  204G   9%  /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
| 625.x264_s(base) 657.xz_s(base)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++       | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Platinum 8280L, 2.70GHz)

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### Compiler Version Notes (Continued)

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<th>641.leela_s(base)</th>
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Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

### Base Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

### Base Portability Flags

| 600.perlbench_s: -DSPEC_LP64  -DSPEC_LINUX_X64 |
| 602.gcc_s: -DSPEC_LP64        |
| 605.mcf_s: -DSPEC_LP64       |
| 620.omnetpp_s: -DSPEC_LP64   |
| 623.xalanchmk_s: -DSPEC_LP64 -DSPEC_LINUX |
| 625.x264_s: -DSPEC_LP64      |
| 631.deepsjeng_s: -DSPEC_LP64 |
| 641.leela_s: -DSPEC_LP64     |
| 648.exchange2_s: -DSPEC_LP64 |
| 657.xz_s: -DSPEC_LP64       |
**SPEC CPU®2017 Integer Speed Result**

**Cisco Systems**  
Cisco UCS C220 M5 (Intel Xeon Platinum 8280L, 2.70GHz)

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

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<th>Test Date:</th>
<th>Sep-2019</th>
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<td>Hardware Availability:</td>
<td>Apr-2019</td>
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<tr>
<td>Software Availability:</td>
<td>May-2019</td>
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**Base Optimization Flags**

**C benchmarks:**  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

**C++ benchmarks:**  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

**Fortran benchmarks:**  
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4  
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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Originally published on 2019-11-04.