**SPEC CPU®2017 Floating Point Speed Result**

**Cisco Systems**  
Cisco UCS C220 M5 (Intel Xeon Platinum 8253, 2.20GHz)

**SPECspeed®2017_fp_base =**

**SPECspeed®2017_fp_peak =**

<table>
<thead>
<tr>
<th>Threads</th>
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</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td></td>
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<tr>
<td>607.cactuBSSN_s</td>
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<tr>
<td>619.lbm_s</td>
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<tr>
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<tr>
<td>627.cam4_s</td>
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<td></td>
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<tr>
<td>644.nab_s</td>
<td></td>
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<tr>
<td>649.fotonik3d_s</td>
<td></td>
</tr>
<tr>
<td>654.roms_s</td>
<td></td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Platinum 8253  
  - **Max MHz:** 3000  
  - **Nominal:** 2200  
  - **Enabled:** 32 cores, 2 chips  
  - **Orderable:** 1,2 Chips  
  - **Cache L1:** 32 KB I + 32 KB D on chip per core  
  - **L2:** 1 MB I+D on chip per core  
  - **L3:** 22 MB I+D on chip per chip  
  - **Other:** None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
- **Storage:** 1 x 1.9 TB SSD SAS  
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** Yes  
- **Firmware:** Version 4.0.4g released Jul-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** None  
- **Power Management:** --

**SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.**
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
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</table>

SPECspeed®2017_fp_base =
SPECspeed®2017_fp_peak =

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8253, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-diml Fri Sep 20 10:15:16 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz
- "physical id"s (chips)
  "physical id"s (chips)
  32 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following
  exerts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 16
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 32

(Continued on next page)
**SPEC CPU®2017 Floating Point Speed Result**

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**Cisco Systems**

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| SPECspeed®2017_fp_base = |
| SPECspeed®2017_fp_peak = |

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**CPU2017 License:** 9019  
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**Platform Notes (Continued)**

- On-line CPU(s) list: 0-31
- Thread(s) per core: 1
- Core(s) per socket: 16
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz
- Stepping: 6
- CPU MHz: 2200.000
- CPU max MHz: 3000.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 4400.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 22528K
- NUMA node0 CPU(s): 0-15
- NUMA node1 CPU(s): 16-31

**Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp nonstop_tsc cpuid aperf perfPref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ecc cat_13 cdp_13 invpcid_single intel_patin mba tpr_shadow vnmi flexpriority ept vptid fsgsbase tsc_adjust bmon hle avx2 smep bmi2 erms invpcid rtm cmq mxp rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsave xsaveopt xsavec xsaveopt cqm_1 cqm_2 cqm_4 cqm_8 cqm_16 cqm_64 cqm_128 cqm_mbm_total cqm_mbm_local ibpb ibrs ibrs ibrs ibrs dtherm ida arat pfn hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data

cache size : 22528 KB

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Platform Notes (Continued)

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 385605 MB
node 0 free: 381270 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 387056 MB
node 1 free: 386534 MB
node distances:
node   0   1
0:  10  21
1:  21  10

From /proc/meminfo

MemTotal:       791206084 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-diml 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
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Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

(Continued on next page)
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Base Compiler Invocation (Continued)

Benchmarks using Fortran, C, and C++:
```
icpc -m64 icc -m64 -std=c11 lnk -m64
```

Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
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<tr>
<td>621.wrf_s</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian</td>
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</tr>
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<td>628.pop2_s</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl</td>
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</table>

Base Optimization Flags

C benchmarks:
```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
```

Fortran benchmarks:
```
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs
```

Benchmarks using both Fortran and C:
```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
```

(Continued on next page)
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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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