## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**  
Cisco UCS C220 M5 (Intel Xeon Gold 6252, 2.10GHz)  

<table>
<thead>
<tr>
<th>threads</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
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<tbody>
<tr>
<td>48</td>
<td>9.95</td>
<td>10.2</td>
</tr>
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</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Sep-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Hardware

- **CPU Name:** Intel Xeon Gold 6252  
  - Max MHz: 3700  
  - Nominal: 2100  
  - Enabled: 48 cores, 2 chips  
  - Orderable: 1.2 Chips  
  - Cache L1: 32 KB I + 32 KB D on chip per core  
  - L2: 1 MB I+D on chip per core  
  - L3: 35.75 MB I+D on chip per chip  
  - Other: None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
- **Storage:** 1 x 1.9 TB SSD SAS  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
  - 4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** Yes  
- **Firmware:** Version 4.0.4g released Jul-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** --
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### Results Table

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<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
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<tr>
<td>600.perlbench_s</td>
<td>48</td>
<td>271</td>
<td>6.55</td>
<td>271</td>
<td>6.55</td>
<td>272</td>
<td>6.52</td>
<td>272</td>
<td>6.52</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>48</td>
<td>388</td>
<td>8.22</td>
<td>388</td>
<td>8.22</td>
<td>388</td>
<td>8.22</td>
<td>388</td>
<td>8.22</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>48</td>
<td>187</td>
<td>8.71</td>
<td>184</td>
<td>8.84</td>
<td>182</td>
<td>8.98</td>
<td>181</td>
<td>8.99</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>48</td>
<td>120</td>
<td>11.8</td>
<td>120</td>
<td>11.8</td>
<td>120</td>
<td>11.8</td>
<td>120</td>
<td>11.8</td>
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<td>48</td>
<td>127</td>
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<td>127</td>
<td>13.9</td>
<td>127</td>
<td>13.9</td>
<td>126</td>
<td>13.9</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>48</td>
<td>273</td>
<td>5.25</td>
<td>273</td>
<td>5.25</td>
<td>272</td>
<td>5.27</td>
<td>273</td>
<td>5.25</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>48</td>
<td>376</td>
<td>4.53</td>
<td>377</td>
<td>4.53</td>
<td>377</td>
<td>4.52</td>
<td>376</td>
<td>4.54</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>48</td>
<td>186</td>
<td>15.8</td>
<td>186</td>
<td>15.8</td>
<td>186</td>
<td>15.8</td>
<td>186</td>
<td>15.8</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>48</td>
<td>273</td>
<td>23.0</td>
<td>273</td>
<td>23.0</td>
<td>268</td>
<td>23.0</td>
<td>268</td>
<td>23.0</td>
</tr>
</tbody>
</table>

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default
- Prior to runcpu invocation
- Filesystem page cache synced and cleared with:
  - sync; echo 3> /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6252, 2.10GHz)

SPECspeed®2017_int_base = 9.95
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Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-jm4k Thu Sep 26 16:24:47 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6252 CPU @ 2.10GHz
 2 "physical id"s (chips)
 48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6252 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

(Continued on next page)
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Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-23
NUMA node1 CPU(s): 24-47
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdmsr
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
apicrmrr mtrrpst tsc_known_freq pni clflushopt dtc64 monitor ds_cpl vmx smx est tm2 ssse3
sdm vmptrunc vsfn vmpost fpstitch vsx86m vsx86m2 fbrk pht pdmAtomic fpu_exception
pmx sxvms wp pmx_dir pxum c26 cmea msr_perf easiest msr_perf_counter

From /proc/cpuinfo cache data
  cache size: 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
  physical chip.

  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
  node 0 size: 385608 MB
  node 0 free: 384966 MB
  node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
  node 1 size: 387059 MB
  node 1 free: 386564 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 791212372 KB
  HugePages_Total: 0
  Hugepagesize: 2048 KB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"

(Continued on next page)
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Platform Notes (Continued)

ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
 Linux linux-jm4k 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
 x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 26 16:21

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb1 xfs 224G 20G 204G 9% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

===============================================
C    | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
===============================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

===============================================
C++  | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
===============================================

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
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Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

(Continued on next page)
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**Base Optimization Flags (Continued)**

C benchmarks (continued):
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

C++ benchmarks:
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4`  
  `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc`

Fortran benchmarks:
- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -nostandard-realloc-lhs`

---

**Peak Compiler Invocation**

C benchmarks:
- `icc -m64 -std=c11`

C++ benchmarks:
- `icpc -m64`

Fortran benchmarks:
- `ifort -m64`

---

**Peak Portability Flags**

Same as Base Portability Flags

---

**Peak Optimization Flags**

C benchmarks:
- `600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2`  
  `-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3`  
  `-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp`  
  `-DSPEC_OPENMP -fno-strict-overflow`  
  `-L/usr/local/je5.0.1-64/lib -ljemalloc`

- `602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2`  
  `-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3`

(Continued on next page)
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Peak Optimization Flags (Continued)

602.gcc_s (continued):
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

631.deepsjeng_s: Same as 623.xalancbmk_s
641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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