## SPEC CPU®2017 Integer Rate Result

### Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6244, 3.60GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>SPECrate®2017_int_base = 134</th>
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</tr>
</thead>
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<td></td>
</tr>
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<td></td>
</tr>
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Copies</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>32</td>
</tr>
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</table>

### CPU Name:
Intel Xeon Gold 6244
Max MHz: 4400
Nominal: 3600
Enabled: 16 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 1.9 TB SSD SAS
Other: None

### Other:
jemalloc memory allocator V5.0.1
Power Management: --
Cisco Systems
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Results Table

<table>
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<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>32</td>
<td>511</td>
<td>99.6</td>
<td>510</td>
<td>100</td>
<td>509</td>
<td>100</td>
<td>32</td>
<td>449</td>
<td>113</td>
<td>448</td>
<td>114</td>
<td>451</td>
<td>113</td>
<td></td>
<td></td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>32</td>
<td>410</td>
<td>111</td>
<td>410</td>
<td>111</td>
<td>409</td>
<td>111</td>
<td>32</td>
<td>362</td>
<td>125</td>
<td>363</td>
<td>125</td>
<td>362</td>
<td>125</td>
<td></td>
<td></td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>32</td>
<td>285</td>
<td>181</td>
<td>285</td>
<td>181</td>
<td>287</td>
<td>180</td>
<td>32</td>
<td>284</td>
<td>182</td>
<td>285</td>
<td>181</td>
<td>287</td>
<td>180</td>
<td></td>
<td></td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>32</td>
<td>530</td>
<td>79.2</td>
<td>531</td>
<td>79.1</td>
<td>533</td>
<td>78.8</td>
<td>32</td>
<td>532</td>
<td>79.0</td>
<td>530</td>
<td>79.2</td>
<td>531</td>
<td>79.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>32</td>
<td>203</td>
<td>167</td>
<td>200</td>
<td>169</td>
<td>201</td>
<td>168</td>
<td>32</td>
<td>196</td>
<td>173</td>
<td>196</td>
<td>172</td>
<td>196</td>
<td>173</td>
<td></td>
<td></td>
</tr>
<tr>
<td>525.x264_r</td>
<td>32</td>
<td>203</td>
<td>276</td>
<td>204</td>
<td>275</td>
<td>204</td>
<td>275</td>
<td>32</td>
<td>195</td>
<td>288</td>
<td>194</td>
<td>288</td>
<td>195</td>
<td>288</td>
<td></td>
<td></td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>32</td>
<td>334</td>
<td>110</td>
<td>334</td>
<td>110</td>
<td>334</td>
<td>110</td>
<td>32</td>
<td>335</td>
<td>109</td>
<td>334</td>
<td>110</td>
<td>334</td>
<td>110</td>
<td></td>
<td></td>
</tr>
<tr>
<td>541.leela_r</td>
<td>32</td>
<td>516</td>
<td>103</td>
<td>518</td>
<td>102</td>
<td>508</td>
<td>104</td>
<td>32</td>
<td>509</td>
<td>104</td>
<td>509</td>
<td>104</td>
<td>508</td>
<td>104</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>32</td>
<td>310</td>
<td>270</td>
<td>310</td>
<td>270</td>
<td>310</td>
<td>270</td>
<td>32</td>
<td>310</td>
<td>270</td>
<td>311</td>
<td>270</td>
<td>311</td>
<td>270</td>
<td></td>
<td></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>32</td>
<td>414</td>
<td>83.5</td>
<td>414</td>
<td>83.4</td>
<td>414</td>
<td>83.4</td>
<td>32</td>
<td>414</td>
<td>83.5</td>
<td>415</td>
<td>83.4</td>
<td>414</td>
<td>83.6</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
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SPECrate®2017_int_base = 134
SPECrate®2017_int_peak = 139

General Notes (Continued)

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcd8f2999c33d61f64985e4585ea9
running on linux-3yo3 Fri Sep 27 18:17:10 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6244 CPU @ 3.60GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 2 17 18 19 20 24 25
physical 1: cores 2 3 4 8 9 11 17 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6244 CPU @ 3.60GHz
Stepping: 6
CPU MHz: 3600.000

(Continued on next page)
SPEC CPU®2017 Integer Rate Result
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Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

CPU max MHz: 4400.0000
CPU min MHz: 1200.0000
BogoMIPS: 7200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0,2,6,7,16,18,22,23
NUMA node1 CPU(s): 1,3-5,17,19-21
NUMA node2 CPU(s): 8,11,12,14,24,27,28,30
NUMA node3 CPU(s): 9,10,13,15,25,26,29,31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperf perfctr tsc_known_freq pni pclmulqdq dtel64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt

From numactl --hardware

```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

/proc/cpuinfo cache data

```
cache size: 25344 KB
```

(Continued on next page)
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Platform Notes (Continued)

2:  21  21  10  11
3:  21  21  11  10

From /proc/meminfo
MemTotal:       791206252 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-3yo3 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown):          Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 27 18:14

SPEC is set to: /home/cpu2017
  Filesystem  Type  Size  Used Avail Use% Mounted on
  /dev/sda1    xfs   224G  20G  204G  9% /

Additional information from dmidecode follows.  WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
  Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
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Compiler Version Notes

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<th>Notes</th>
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</table>
| C        | 502.gcc_r(peak) | Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
|          |          | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
|          |          | Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 |
|          |          | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
| C++      | 523.xalancbmk_r(peak) | Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416 |
|          |          | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
|          |          | Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |

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</thead>
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<tr>
<td>C++</td>
<td>523.xalancbmk_r(peak)</td>
</tr>
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<td></td>
</tr>
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</tr>
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<td></td>
</tr>
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</tr>
</tbody>
</table>

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</tr>
</thead>
<tbody>
<tr>
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<td></td>
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</table>

---

### Base Compiler Invocation

- **C benchmarks:**  
  `icc -m64 -std=c11`

- **C++ benchmarks:**  
  `icpc -m64`

- **Fortran benchmarks:**  
  `ifort -m64`

---

### Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
```

---

(Continued on next page)
Base Portability Flags (Continued)

502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

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Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

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### Cisco Systems

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**SPECrate®2017_int_base = 134**

**SPECrate®2017_int_peak = 139**

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**Peak Optimization Flags (Continued)**

**C++ benchmarks:**

- `520.omnetpp_r`: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=4
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc`

- `523.xalancbkmk_r`: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
  -L/usr/local/je5.0.1-32/lib -ljemalloc`

- `531.deepsjeng_r`: Same as `520.omnetpp_r`

- `541.leela_r`: Same as `520.omnetpp_r`

**Fortran benchmarks:**

- `520.omnetpp_r`: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc`

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The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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