Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6240M, 2.60GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base = 10.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_peak = Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Sep-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_int_base (10.1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>36</td>
<td></td>
</tr>
<tr>
<td>600.perbench_s</td>
<td>6.82</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>9.74</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>12.6</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>7.70</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>12.4</td>
</tr>
<tr>
<td>626.xz_s</td>
<td>14.1</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>5.49</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>4.78</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>16.6</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>23.1</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 6240M
- **Max MHz:** 3900
- **Nominal:** 2600
- **Enabled:** 36 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 24.75 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4g released Jul-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --
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SPECspeed®2017_int_peak = Not Run

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-3yo3 Fri Sep 20 07:26:24 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6240M CPU @ 2.60GHz
  2 "physical id"s (chips)
  36 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
  siblings : 18
  physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 36
On-line CPU(s) list: 0-35
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240M CPU @ 2.60GHz
Stepping: 7
CPU MHz: 2600.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

(Continued on next page)
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**SPECspeed®2017_int_base = 10.1**

**SPECspeed®2017_int_peak = Not Run**

Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-17
NUMA node1 CPU(s): 18-35
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_13 invpcid_single intel_pinn mba tpr_shadow vmni flexpriority ept
vpid fsgsbase tsc_adjust bm1 hle avx2 smep bmi2 erms invpcid rtm cqm mx mpx rdts_a
avx512f avx512dq rdseed adx smap clflushopt clwb intelep va avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mmb_total cqm_mmb_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
node 0 size: 385634 MB
node 0 free: 384941 MB
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
node 1 size: 387027 MB
node 1 free: 386639 MB
node distances:
node 0 1
  0: 10 21
  1: 21 10

From /proc/meminfo

MemTotal: 791205816 KB
HugePages_Total: 0
Hugepagesize: 2048 KB

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"

(Continued on next page)
## Platform Notes (Continued)

```bash
cpe_name="cpe:/o:suse:sles:15"
```

```bash
uname -a:
    Linux linux-3yo3 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- CVE-2017-5754 (Meltdown): Not affected
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 20 07:20

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda1</td>
<td>xfs</td>
<td>224G</td>
<td>20G</td>
<td>204G</td>
<td>9%</td>
<td>/</td>
</tr>
</tbody>
</table>

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
- Memory: 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

## Compiler Version Notes

```bash
C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
        | 625.x264_s(base) 657.xz_s(base)
---------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
---------------
C++     | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
        | 641.leela_s(base)
---------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
```
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| Test Date: Sep-2019 |
| Hardware Availability: Apr-2019 |
| Software Availability: May-2019 |

Compiler Version Notes (Continued)

Copyright 1985-2019 Intel Corporation. All rights reserved.

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Fortran | 648.exchange2_s(base)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
---

Base Compiler Invocation

C benchmarks:
`icc -m64 -std=c11`

C++ benchmarks:
`icpc -m64`

Fortran benchmarks:
`ifort -m64`

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
`-Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

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Base Optimization Flags (Continued)

C benchmarks (continued):
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local//IntelCompiler19//compilers_and_libraries_2019.4.227//linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-09-19 21:56:23-0400.
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