### Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5215M, 2.50GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 123</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak = 127</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Sep-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

---

### Hardware

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon Gold 5215M</td>
</tr>
<tr>
<td>Max MHz</td>
<td>3400</td>
</tr>
<tr>
<td>Nominal</td>
<td>2500</td>
</tr>
<tr>
<td>Enabled</td>
<td>20 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3</td>
<td>13.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
<tr>
<td>Memory</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)</td>
</tr>
<tr>
<td>Storage</td>
<td>1 x 1.9 TB SSD SAS</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
</tbody>
</table>

### Software

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS</td>
<td>SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
</tr>
<tr>
<td>Compiler</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel</td>
<td>No</td>
</tr>
<tr>
<td>Firmware</td>
<td>Version 4.0.4g released Jul-2019</td>
</tr>
<tr>
<td>File System</td>
<td>xfs</td>
</tr>
<tr>
<td>System State</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other</td>
<td>jemalloc memory allocator V5.0.1</td>
</tr>
<tr>
<td>Power Management</td>
<td>--</td>
</tr>
</tbody>
</table>
Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>40</td>
<td>692</td>
<td>92.0</td>
<td>688</td>
<td>92.5</td>
<td>687</td>
<td>92.6</td>
<td>40</td>
<td>597</td>
<td>107</td>
<td>598</td>
<td>107</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>40</td>
<td>566</td>
<td>100</td>
<td>562</td>
<td>101</td>
<td>561</td>
<td>101</td>
<td>40</td>
<td>496</td>
<td>114</td>
<td>499</td>
<td>114</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>40</td>
<td>393</td>
<td>165</td>
<td>395</td>
<td>164</td>
<td>393</td>
<td>164</td>
<td>40</td>
<td>393</td>
<td>165</td>
<td>395</td>
<td>164</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>40</td>
<td>647</td>
<td>81.1</td>
<td>646</td>
<td>81.2</td>
<td>646</td>
<td>81.3</td>
<td>40</td>
<td>648</td>
<td>81.0</td>
<td>644</td>
<td>81.5</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>40</td>
<td>296</td>
<td>143</td>
<td>296</td>
<td>143</td>
<td>298</td>
<td>142</td>
<td>40</td>
<td>276</td>
<td>153</td>
<td>276</td>
<td>153</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>40</td>
<td>298</td>
<td>235</td>
<td>298</td>
<td>235</td>
<td>298</td>
<td>235</td>
<td>40</td>
<td>286</td>
<td>245</td>
<td>285</td>
<td>246</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>40</td>
<td>453</td>
<td>101</td>
<td>454</td>
<td>101</td>
<td>453</td>
<td>101</td>
<td>40</td>
<td>453</td>
<td>101</td>
<td>453</td>
<td>101</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>40</td>
<td>710</td>
<td>93.3</td>
<td>714</td>
<td>92.8</td>
<td>710</td>
<td>93.3</td>
<td>40</td>
<td>710</td>
<td>93.3</td>
<td>714</td>
<td>92.8</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>40</td>
<td>428</td>
<td>245</td>
<td>427</td>
<td>246</td>
<td>428</td>
<td>245</td>
<td>40</td>
<td>427</td>
<td>245</td>
<td>428</td>
<td>245</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>40</td>
<td>537</td>
<td>80.5</td>
<td>537</td>
<td>80.5</td>
<td>537</td>
<td>80.4</td>
<td>40</td>
<td>536</td>
<td>80.5</td>
<td>537</td>
<td>80.5</td>
</tr>
</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5.
Transparent Huge Pages enabled by default.
Prior to runcpu invocation:
Filesyste p page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5215M, 2.50GHz)

SPECrate®2017_int_base = 123
SPECrate®2017_int_peak = 127

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bced8f2999c33d61f64985e45859ea9
running on linux-diml Sat Sep 21 22:56:22 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5215M CPU @ 2.50GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 10
  siblings : 20
  physical 0: cores 0 1 2 3 4 8 9 10 11 12
  physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5215M CPU @ 2.50GHz
Stepping: 6
CPU MHz: 2500.000

(Continued on next page)
### SPEC CPU®2017 Integer Rate Result

**Cisco Systems**  
Cisco UCS C220 M5 (Intel Xeon Gold 5215M, 2.50GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>123</td>
<td>127</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Sponsor</th>
<th>Tested by</th>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
</table>

**Platform Notes (Continued)**

- CPU max MHz: 3400.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 5000.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 14080K
- NUMA node0 CPU(s): 0-9,20-29
- NUMA node1 CPU(s): 10-19,30-39
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_i3 cd p13 invpcid_single intel_pinn mba trp_shadow vmx f16e tsc_adjust bmi bmi2 asei mle cmvt Yamal xsavecf xsaveopt xsaves xsaveopt accessordova ftx ftx_64 mrsqm aesni rdrand idapkgarch skgxcp cpuid_fault epb cat_i3 cd p13 invpcid_single intel_pinn mba trp_shadow vmx f16e tsc_adjust bmi bmi2 asei mle cmvt Yamal xsavecf xsaveopt xsaves xsaveopt accessordova ftx ftx_64 mrsqm aesni rdrand idapkgarch skgxcp

```
/proc/cpuinfo cache data
  cache size : 14080 KB
```

From numactl --hardware  
**WARNING:** a numactl 'node' might or might not correspond to a physical chip.
- available: 2 nodes (0-1)
- node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
- node 0 size: 385604 MB
- node 0 free: 384981 MB
- node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
- node 1 size: 387056 MB
- node 1 free: 386608 MB
- node distances:
  - node 0 1
  - 0: 10 21
  - 1: 21 10

From /proc/meminfo
- MemTotal: 791204540 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
- os-release:

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5215M, 2.50GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 123
SPECrate®2017_int_peak = 127

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-diml 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 21 22:55

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 224G 20G 204G 9% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C       | 502.gcc_r(peak) |
|────────|───────────────|
| Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5215M, 2.50GHz)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

| SPECrate®2017_int_base | = 123 |
| SPECrate®2017_int_peak | = 127 |

Cisco Systems

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

---

Compiler Version Notes (Continued)

<table>
<thead>
<tr>
<th>TESTS</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)</td>
<td></td>
</tr>
</tbody>
</table>
|       | Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
|       | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
|       | Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
|       | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
| C++   | 523.xalancbmk_r(peak) |
|       | Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
|       | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
| C++   | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak) |
|       | Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
|       | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
| C++   | 523.xalancbmk_r(peak) |
|       | Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version |

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5215M, 2.50GHz)

SPECrates®2017_int_base = 123
SPECrates®2017_int_peak = 127

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Compiler Version Notes (Continued)

19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---------------------------------------------------------------------

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
     | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
---------------------------------------------------------------------

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---------------------------------------------------------------------

Fortran | 548.exchange2_r(base, peak)
---------------------------------------------------------------------

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5215M, 2.50GHz)

SPEC CPU®2017 Integer Rate Result

<table>
<thead>
<tr>
<th>Test Sponsor</th>
<th>Tested by</th>
<th>CPU2017 License</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cisco Systems</td>
<td>Cisco Systems</td>
<td>9019</td>
<td>Apr-2019</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

SPECrate®2017_int_base = 123
SPECrate®2017_int_peak = 127

Base Portability Flags (Continued)

557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc  -m64  -std=c11

502.gcc_r icc  -m32  -std=c11  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

C++ benchmarks (except as noted below):
icpc  -m64

523.xalancbmk_r icpc  -m32  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort  -m64
## Peak Portability Flags

- **500.perlbench_r**: -DSPEC_LP64 -DSPEC_LINUX_X64  
- **502.gcc_r**: -D_FILE_OFFSET_BITS=64  
- **505.mcf_r**: -DSPEC_LP64  
- **520.omnetpp_r**: -DSPEC_LP64  
- **523.xalancbmk_r**: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
- **525.x264_r**: -DSPEC_LP64  
- **531.deepsjeng_r**: -DSPEC_LP64  
- **541.leela_r**: -DSPEC_LP64  
- **548.exchange2_r**: -DSPEC_LP64  
- **557.xz_r**: -DSPEC_LP64

## Peak Optimization Flags

### C benchmarks:

- **500.perlbench_r**: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
  -fno-strict-overflow  
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
  -lqkmalloc

- **502.gcc_r**: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
  -L/usr/local/je5.0.1-32/lib  
  -ljemalloc

- **505.mcf_r**: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-mem-layout-trans=4  
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
  -lqkmalloc

- **525.x264_r**: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-mem-layout-trans=4  
  -fno-alias  
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
  -lqkmalloc

- **557.xz_r**: Same as 505.mcf_r

### C++ benchmarks:

- **520.omnetpp_r**: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-mem-layout-trans=4  
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
  -lqkmalloc
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5215M, 2.50GHz)

SPECrate®2017_int_base = 123
SPECrate®2017_int_peak = 127

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Optimization Flags (Continued)

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product
names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-09-21 13:26:21-0400.
Originally published on 2019-11-04.