SPEC CPU®2017 Floating Point Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL560 Gen10
(2.30 GHz, Intel Xeon Gold 5218)

SPECrate®2017_fp_base = 355

SPECrate®2017_fp_peak = Not Run

**CPU2017 License:** 3  
**Test Date:** Sep-2019  
**Test Sponsor:** HPE  
**Tested by:** HPE  
**Hardware Availability:** Apr-2019

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>355</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Copies</th>
<th>503.bwaves_r</th>
<th>507.cactuBSSN_r</th>
<th>508.namd_r</th>
<th>510.parest_r</th>
<th>511.povray_r</th>
<th>519.lbm_r</th>
<th>521.wrf_r</th>
<th>526.blender_r</th>
<th>527.cam4_r</th>
<th>538.imagick_r</th>
<th>544.nab_r</th>
<th>549.fotonik3d_r</th>
<th>554.roms_r</th>
</tr>
</thead>
<tbody>
<tr>
<td>128</td>
<td>297</td>
<td>262</td>
<td>202</td>
<td>414</td>
<td>209</td>
<td>392</td>
<td>365</td>
<td>294</td>
<td>365</td>
<td>768</td>
<td>571</td>
<td>165</td>
<td></td>
</tr>
</tbody>
</table>

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-150.32-default
- **Compiler:** C/C++: Version 19.0.2.187 of Intel C/C++ Compiler Build 20190117 for Linux;
  Fortran: Version 19.0.2.187 of Intel Fortran Compiler Build 20190117 for Linux
- **Parallel:** No
- **Firmware:** HPE BIOS Version U34 02/02/2019 released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --

**Hardware**

- **CPU Name:** Intel Xeon Gold 5218
- **Max MHz:** 3900
- **Nominal:** 2300
- **Enabled:** 64 cores, 4 chips, 2 threads/core
- **Orderable:** 1, 2, 4 chip(s)
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 22 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2933Y-R, running at 2666)
- **Storage:** 1 x 480 GB SAS SSD, RAID 0
- **Other:** None
### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>128</td>
<td>1419</td>
<td>905</td>
<td>1419</td>
<td>904</td>
<td>1418</td>
<td>905</td>
<td></td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>128</td>
<td>546</td>
<td>297</td>
<td>546</td>
<td>297</td>
<td>546</td>
<td>297</td>
<td></td>
<td></td>
</tr>
<tr>
<td>508.namd_r</td>
<td>128</td>
<td>463</td>
<td>263</td>
<td>463</td>
<td>262</td>
<td>464</td>
<td>262</td>
<td></td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td>128</td>
<td>1658</td>
<td>202</td>
<td>1655</td>
<td>202</td>
<td>1658</td>
<td>202</td>
<td></td>
<td></td>
</tr>
<tr>
<td>511.povray_r</td>
<td>128</td>
<td>723</td>
<td>414</td>
<td>722</td>
<td>414</td>
<td>723</td>
<td>413</td>
<td></td>
<td></td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>128</td>
<td>647</td>
<td>209</td>
<td>646</td>
<td>209</td>
<td>647</td>
<td>209</td>
<td></td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>128</td>
<td>732</td>
<td>392</td>
<td>730</td>
<td>393</td>
<td>736</td>
<td>390</td>
<td></td>
<td></td>
</tr>
<tr>
<td>526.blender_r</td>
<td>128</td>
<td>507</td>
<td>385</td>
<td>506</td>
<td>385</td>
<td>507</td>
<td>385</td>
<td></td>
<td></td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>128</td>
<td>614</td>
<td>365</td>
<td>615</td>
<td>364</td>
<td>607</td>
<td>369</td>
<td></td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>128</td>
<td>412</td>
<td>773</td>
<td>414</td>
<td>768</td>
<td>414</td>
<td>768</td>
<td></td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td>128</td>
<td>373</td>
<td>577</td>
<td>377</td>
<td>571</td>
<td>378</td>
<td>570</td>
<td></td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>128</td>
<td>1698</td>
<td>294</td>
<td>1696</td>
<td>294</td>
<td>1695</td>
<td>294</td>
<td></td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>128</td>
<td>1232</td>
<td>165</td>
<td>1230</td>
<td>165</td>
<td>1231</td>
<td>165</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

### General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH="/cpu2017/lib/ia32:/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9–7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL560 Gen10
(2.30 GHz, Intel Xeon Gold 5218)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>355</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

General Notes (Continued)

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Configuration:
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Throughput Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Performance
Advanced Memory Protection set to Advanced ECC
Sub-NUMA Clustering set to Disabled
Sysinfo program /cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on consip Tue Sep 24 15:35:36 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
- 4 "physical id"s (chips)
- 128 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores : 16
  - siblings : 32
  - physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  - physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  - physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  - physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL560 Gen10
(2.30 GHz, Intel Xeon Gold 5218)

SPECrate®2017_fp_base = 355
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: Aug-2019

Platform Notes (Continued)

Byte Order: Little Endian
CPU(s): 128
On-line CPU(s) list: 0-127
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
Stepping: 6
CPU MHz: 2300.000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-15, 64-79
NUMA node1 CPU(s): 16-31, 80-95
NUMA node2 CPU(s): 32-47, 96-111
NUMA node3 CPU(s): 48-63, 112-127
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acp1 mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpoe gb rdtscp
lm constant tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop tsc cpl aperf
mpn fcpl pmlnul dq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrr pdcm pcd dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat _ld cdp _ld
invpcid_single intel_pmm innb mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bni l he avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rsseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaveav cxsave qcache l1c qcache l2c
qcache_l3_total qcache_mbb_local dtherm ida arat pln pts pkp ospke avx512_vnni md clear
flush lld arch_capabilities

/cache/cpulinfo cache data
  cache size: 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 64 65 66 67 68 69 70 71 72 73 74 75
  76 77 78 79
  node 0 size: 386580 MB
  node 0 free: 365668 MB
  node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 80 81 82 83 84 85 86 87 88

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL560 Gen10
(2.30 GHz, Intel Xeon Gold 5218)

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

SPECrater®2017_fp_base = 355
SPECrater®2017_fp_peak = Not Run

Platform Notes (Continued)

89 90 91 92 93 94 95
node 1 size: 387065 MB
node 1 free: 376726 MB
node 2 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 96 97 98 99 100 101 102
103 104 105 106 107 108 109 110 111
node 2 size: 387065 MB
node 2 free: 377463 MB
node 3 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 112 113 114 115 116 117
118 119 120 121 122 123 124 125 126 127
node 3 size: 386827 MB
node 3 free: 377140 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10

From /proc/meminfo
MemTotal: 1584679516 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
"os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux consip 4.12.14-150.32-default #1 SMP Thu Aug 1 08:42:52 UTC 2019 (a2a3983)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
run-level 3 Sep 23 14:29

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL560 Gen10
(2.30 GHz, Intel Xeon Gold 5218)

SPECrat®2017_fp_base = 355
SPECrat®2017_fp_peak = Not Run

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Platform Notes (Continued)

SPEC is set to: /cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda4 btrfs 444G 138G 306G 31% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS HPE U34 02/02/2019
Memory:
48x UNKNOWN NOT AVAILABLE 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base) |
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.2.187 Build 20190117 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |

==============================================================================
| C++              | 508.namd_r(base) 510.parest_r(base) |
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.2.187 Build 20190117 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |

==============================================================================
| C++, C          | 511.povray_r(base) 526.blender_r(base) |
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.2.187 Build 20190117 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |

==============================================================================
| C++, C, Fortran | 507.cactuBSSN_r(base) |

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL560 Gen10
(2.30 GHz, Intel Xeon Gold 5218)

SPECrate®2017_fp_base = 355
SPECrate®2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Date</th>
<th>Test Sponsor</th>
<th>Hardware Availability</th>
<th>Tested by</th>
<th>Software Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Sep-2019</td>
<td>HPE</td>
<td>Apr-2019</td>
<td>HPE</td>
<td>Aug-2019</td>
</tr>
</tbody>
</table>

Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran         | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL560 Gen10
(2.30 GHz, Intel Xeon Gold 5218)

SPECrate®2017_fp_base = 355
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: Aug-2019

Base Compiler Invocation (Continued)

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-convert big_endian

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-convert big_endian

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL560 Gen10
(2.30 GHz, Intel Xeon Gold 5218)

BASE OPTIMIZATION FLAGS (Continued)

Benchmarks using both C and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-09-24 15:35:36-0400.